Theory and Applications of Incremental $\Delta\Sigma$ Converters

János Márkus, *Student Member, IEEE*, José Silva, *Student Member, IEEE*, and Gabor C. Temes, *Life Fellow, IEEE*

***Abstract*—Analog–Digital (A/D) converters used in instrumentation and measurements often require high *absolute* accuracy, including very high linearity and negligible dc offset. The realization of high-resolution Nyquist-rate converters becomes very expensive when the resolution exceeds 16 bits. The conventional delta–sigma ($\Delta\Sigma$) structures used in telecommunication and audio applications usually cannot satisfy the requirements of high absolute accuracy and very small offset. The incremental (or integrating) converter provides a solution for such measurement applications, as it has most advantages of the $\Delta\Sigma$ converter, yet is capable of offset-free and accurate conversion. In this paper, theoretical and practical aspects of higher order incremental converters are discussed. The operating principles, topologies, specialized digital filter design methods, and circuit level issues are all addressed. It is shown how speed, resolution, and A/D complexity can be optimized for a given design, and how with some special digital filters improved speed/resolution ratio can be achieved. The theoretical results are verified by showing design examples and simulation results.**

***Index Terms*—Charge balancing delta–sigma ($\Delta\Sigma$) modulator, decimating filter, dither, incremental (integrating) analog–digital (A/D) converter, no-latency $\Delta\Sigma$ converter, one-shot $\Delta\Sigma$ converter, staggered zeros, switched-capacitor circuit.**

I. Introduction

DELTA–SIGMA ($\Delta\Sigma$) modulation, utilizing oversampling and noise-shaping, is a well-known technique used in high-accuracy analog–digital (A/D) converters. These converters, used mainly in telecommunication and consumer electronics applications, are characterized by their signal-processing parameters, such as dynamic range and signal-to-noise ratio (SNR). Moreover, these converters are mainly dedicated to applications which can tolerate offset and gain errors.

On the other hand, in instrumentation and measurement (such as digital voltmeters and sensor applications) often data converters with high *absolute* accuracy are required, i.e., offset and gain errors cannot be tolerated. These converters are designed to deliver good sample-by-sample conversion performance. They need to exhibit excellent differential and integral linearity, low offset and gain errors, and often, they must have high resolution and low power consumption. In contrast with telecommunication applications, where a running waveform needs to be digitized continuously, and mainly the spectral behavior of the signal is important, in sensor applications the goal is to digitize individual samples or the average value of a noisy dc signal.

Among Nyquist-rate A/D converter (ADCs), dual-slope and voltage-to-frequency converters have dominated dc measurement applications for many years. However, as the need to integrate analog circuits in a low-voltage CMOS environment increased, incremental ADCs (also known as one-shot, no-latency, or charge-balancing $\Delta\Sigma$ converters) became more often used, as these converters can offer superior performance while requiring no external components (such as integrating capacitors). Their tolerance of analog component errors is also a great advantage.

This paper discusses the theory, design, and application of higher order incremental converters. Specialized digital decimating filters are also described for such converters. Finally, simulation results and design examples are described to verify the theory.

The paper is organized as follows. Section II describes the basic operation of the first-order incremental converter. Section III introduces the general higher order $\Delta\Sigma$ modulator topology, and discusses its operation. In Section IV, the digital filter following the modulator is examined. Section V addresses some circuit-level realization problems and their possible solutions. Section VI verifies the methods discussed earlier by describing several examples, with various analog- and digital-circuit complexities, clock frequency, and achievable resolution. Section VII gives the conclusions.

II. Incremental Converters

A. First-Order Incremental Converter

The first-order incremental A/D converter [1] represents a hybrid between a Nyquist-rate dual slope converter [2, ch. 7] and a $\Delta\Sigma$ one [3]. Here, the operation of the unipolar first-order converter is described (Fig. 1). It is similar to that of a dual-slope ADC; the main difference is that there the integration of the input and the reference is performed separately, while here, they are alternating.

At the beginning of a new conversion, the integrator in the loop and the output counter are both reset. Next, a fixed number $(n = 2^{n_{\rm bit}})$ of integration steps are performed (assuming a discrete-time integrator), where $n_{\rm bit}$ is the required resolution in bits. Whenever the input to the comparator exceeds zero, its

Manuscript received May 28, 2003; revised November 28, 2003. This work was supported in part by the National Science Foundation Center for Design of Analog-Digital Integrated Circuits, in part by the National Science Foundation U.S.-Hungary Grant, under Contract UX026A, in part by the Hungarian Fund for Scientific Research, under Contract OTKA T 033 053, and in part by the Siemens AG. This paper was recommended by Associate Editor A. Petralgia.

J. Márkus is with the Department of Measurement and Information Systems, Budapest University of Technology and Economics, H-1521 Budapest, Hungary (e-mail: markus@mit.bme.hu).

J. Silva and G. C. Temes are with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR 97331 USA (e-mail: silva@eecs.oregonstate.edu; temes@eecs.oregonstate.edu).

Digital Object Identifier 10.1109/TCSI.2004.826202

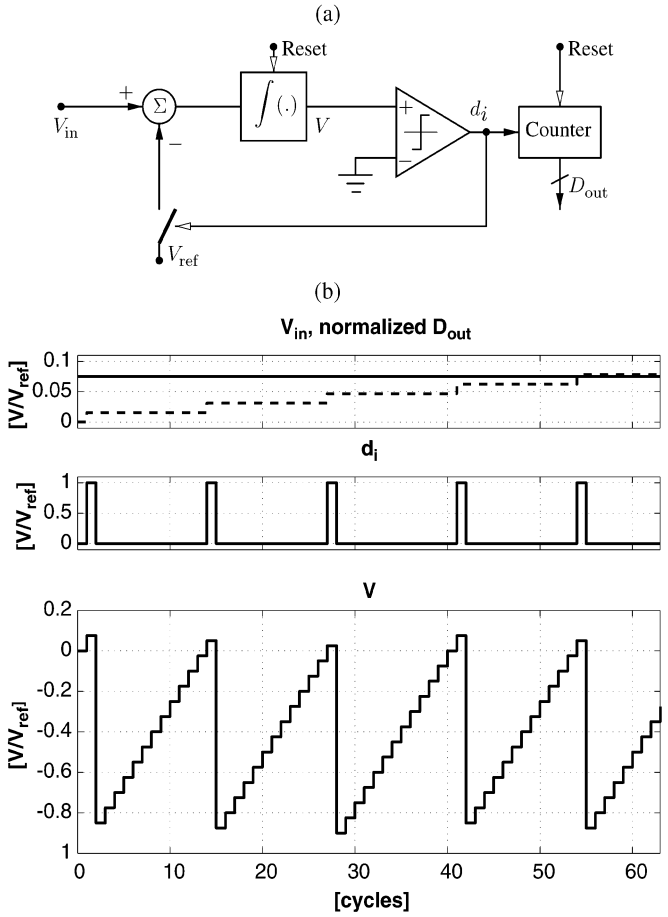


Fig. 1. (a) First-order incremental converter and (b) its waveforms ($n_{\rm bit}$ = 6 bits, $V_{\rm in} = 0.075 V_{\rm ref}$).

output becomes 1, and $-V_{\rm ref}$ is added to the input of the analog integrator. After n steps, the output of the integrator becomes

$$V = nV_{\rm in} - NV_{\rm ref} \tag{1}$$

where N is the number of clock periods when feedback was applied. Since V must satisfy $-V_{\rm ref} < V < V_{\rm in}$, it follows that

$$N = n\left(\frac{V_{\rm in}}{V_{\rm ref}}\right) + \epsilon \tag{2}$$

where $\epsilon \in [-1, 1]$. Generating N with a simple counter at the output of the modulator, one can easily get the digital representation of the input signal. Note that the residual error at the output of the integrator is

$$V = -2e_q V_{\rm ref} \tag{3}$$

where $e_q \in [-0.5, 0.5]$ is the quantization error of the conversion.

Fig. 2 shows the quantization error e_q [Fig. 2(a)] and the output of the integrator $V(n)$ at the end of the conversion [Fig. 2(b)] for a 6-bit bipolar first-order incremental converter, as functions of the input signal. It can be seen that in this case, the quantization error is similar to that of a Nyquist-rate converter, and that (3) is satisfied.

The converter requires only simple analog and digital circuitry, needs no precision components, and can easily be extended to bipolar operation, even using only a single reference. The area and power requirements are also very modest [1].

The incremental converter is structurally similar to the conventional ΔΣ converter, but there are significant differences: 1) the converter does not operate continuously; 2) both the analog and digital integrators are reset after each conversion; and 3) the decimating filter following the ΔΣ modulator can be realized with a much simpler structure (in this case, with a simple counter).

B. Extensions to More Complex Architectures

The first-order incremental converter's biggest drawback is that it is very slow: for n-bit resolution, it needs 2^n clock periods for each conversion cycle. This leads to a very slow conversion rate compared to its clock frequency. To reduce the number of cycles during one conversion, various modifications have been proposed.

In [4], the use of the two-stage (MASH) incremental converter was described, consisting of first-order modulators. In addition, by detecting the sign of V at the end of the conversion, an extra bit of resolution was obtained. Using a two-stage architecture, the number of clock periods required for 16-bit accuracy was reduced to $p = 257$ from the much larger value of 2^{16} needed for the first-order converter. As the circuit cancels the outputs of cascaded stages, it is sensitive to circuit nonidealities such as component mismatches and finite op-amp gains. A similar solution was proposed in [5].

Other researchers used the fact that the quantization error multiplied by 2^n is available at the end of the conversion as an analog signal V [cf. (3)]. As this is a large signal, it can be easily used as part of a digital correction scheme, further refining the conversion's resolution. As an example, [6] digitized the quantization error at the end of each conversion with a Nyquist-rate multibit converter.

In [7], successive approximation was used at the end of the conversion, applying a reduced feedback signal in every step. In [8], an algorithmic converter was introduced in which at the end of the incremental conversion the same hardware was reused for refining the quantization noise, reducing the quantization error by a factor of 2 in every step. In [9], a two-step algorithmic conversion was used, resulting in very low power and reduced chip area.

Another way of extending the resolution of incremental converters is to use higher order single-stage modulators. Even though some commercially available converters [10]–[13] may use such structures, their theory and design methodology seems to be unavailable in the open literature. Among the few relevant publications is [14]. A similar approach, using a digital filter matched exactly to the analog loop filter, was described by Lyden [15], [16].

In Section III, the structure and operation of higher order incremental converters will be discussed.

III. Operation of Higher Order Incremental Converters

The basic block diagram of a higher order incremental converter is shown in Fig. 3. The converter consists of a dis-

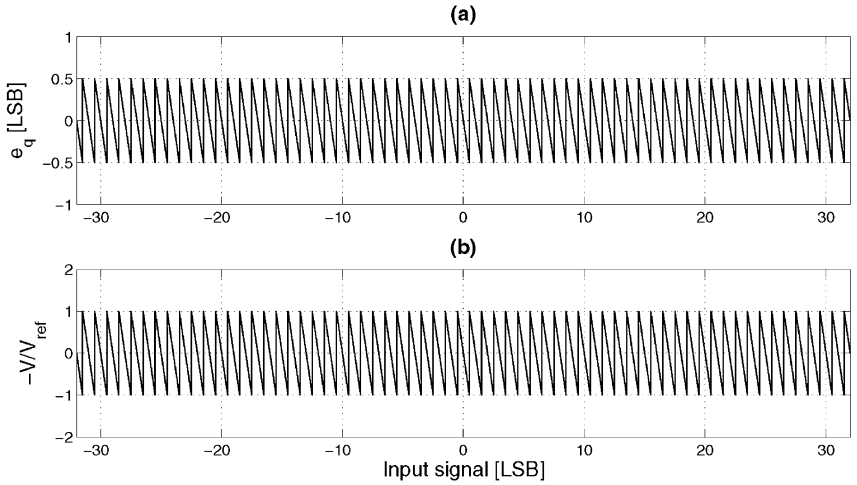


Fig. 2. (a) Quantization error and (b) inverted output of the analog integrator at the end of the conversion of a 6-bit bipolar first-order incremental converter.

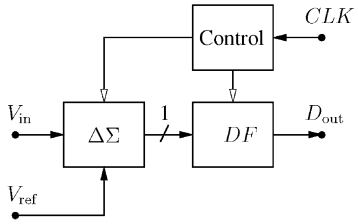


Fig. 3. Block diagram of the higher order incremental converter.

crete-time (e.g., switched-capacitor) $\Delta\Sigma$ modulator, a digital filter DF and a control circuit. The operation will be discussed in terms of a third-order cascaded-integrator/feed-forward (CIFF) modulator structure [17] shown on Fig. 4.

As in the first-order modulator, all memory elements, both analog and digital, must be reset at the beginning of each conversion cycle. Then, $V_{\rm in}$ is applied to the input of the first integrator. Using the notations of Fig. 4, the output signals of all integrators can readily be found in the time domain after the first n clock cycles.

The first integrator's output samples are given by

$$\begin{aligned} V_{i_1}[0] &= 0 \\ V_{i_1}[1] &= b(V_{\rm in}[0] - d_0 V_{\rm ref}) \\ V_{i_1}[2] &= V_{i_1}[1] + b(V_{\rm in}[0] - d_1 V_{\rm ref}) \\ &= b(V_{\rm in}[0] + V_{\rm in}[1] - d_0 V_{\rm ref} - d_1 V_{\rm ref}) \\ &\vdots \\ V_{i_1}[n] &= b\sum_{k=0}^{n-1}(V_{\rm in}[k] - d_k V_{\rm ref}) \end{aligned} \tag{4}$$

where $d_k = \pm 1$ is the comparator output in the kth cycle.

Similarly, the sequence of outputs of the second integrator is

$$\begin{aligned} V_{i_2}[0] &= 0 \\ V_{i_2}[1] &= c_1 V_{i_1}[0] + V_{i_2}[0] = 0 \\ V_{i_2}[2] &= c_1 V_{i_1}[1] + V_{i_2}[1] = c_1(V_{i_1}[1] + V_{i_1}[0]) \\ &\vdots \\ V_{i_2}[n] &= c_1 \sum_{l=0}^{n-1} V_{i_1}[l] = c_1 b \sum_{l=0}^{n-1}\sum_{k=0}^{l-1}(V_{\rm in}[k] - d_k V_{\rm ref}) \end{aligned} \tag{5}$$

and that of the third is

$$\begin{aligned} V_{i_3}[0] &= 0 \\ V_{i_3}[1] &= c_2 V_{i_2}[0] + V_{i_3}[0] = c_2 V_{i_2}[0] = 0 \\ V_{i_3}[2] &= c_2 V_{i_2}[1] + V_{i_3}[1] = c_2(V_{i_2}[1] + V_{i_2}[0]) = 0 \\ &\vdots \\ V_{i_3}[n] &= c_2 \sum_{m=0}^{n-1} V_{i_2}[m] \\ &= c_2 c_1 b \sum_{m=0}^{n-1}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1}(V_{\rm in}[k] - d_k V_{\rm ref}). \end{aligned} \tag{6}$$

In the following, a constant $V_{\rm in}$ is assumed, which can be achieved using a sample-and-hold (S/H) circuit at the input of the converter. A detailed discussion of the operation with a time-varying input (e.g., dc input with added noise or a periodic signal) is given in Section IV.

If the loop is stable for all possible dc inputs, which can be achieved by carefully designing the loop and limiting the maximum gain of the noise transfer function (NTF) [3, Ch. 4–8], [17], then, $V_{i_3}[n]$ in (6) is bounded by $\pm V_{\rm ref}$. Rearranging (6) and assuming a constant $V_{\rm in}$, one gets

$$\sum_{m=0}^{n-1}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1} d_k V_{\rm ref} = \frac{(n-2)(n-1)n}{3!}V_{\rm in} + \frac{V_{i_3}[n]}{c_2 c_1 b} \tag{7}$$

i.e.,

$$\begin{aligned} &-\frac{3!}{(n-2)(n-1)n}\frac{1}{c_2 c_1 b}V_{\rm ref} \\ &< V_{\rm in} - \frac{3!}{(n-2)(n-1)n}V_{\rm ref}\sum_{m=0}^{n-1}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1} d_k \\ &< +\frac{3!}{(n-2)(n-1)n}\frac{1}{c_2 c_1 b}V_{\rm ref}. \end{aligned} \tag{8}$$

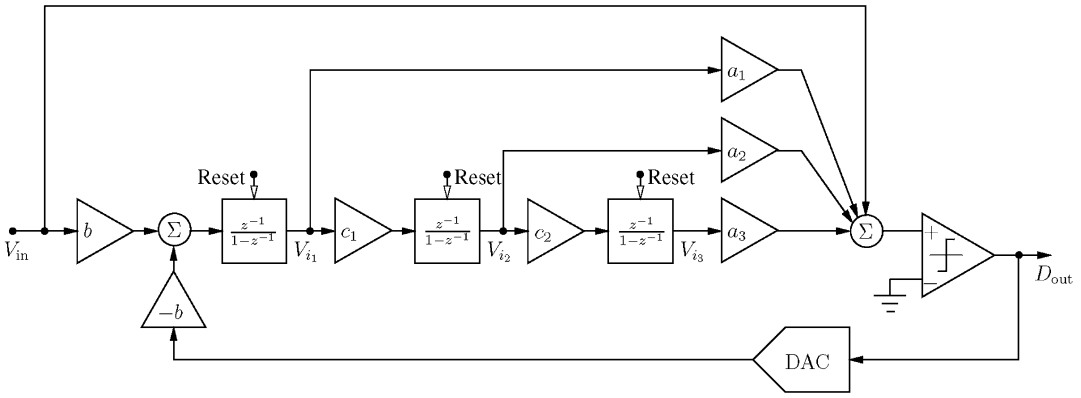


Fig. 4. Third-order CIFF architecture.

Thus, after n clock periods, an estimate of $V_{\text{in}}/V_{\text{ref}}$ can be found as

$$\frac{\hat{V}_{\text{in}}}{V_{\text{ref}}} = \frac{3!}{(n-2)(n-1)n} \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k. \tag{9}$$

From the limits on the error of the estimate of V_{in}, as given in (8), and using the fact that in an ideal ADC these limits are equal to $\pm V_{\text{LSB}}/2$, one can find the equivalent value of the LSB voltage as

$$V_{\text{LSB}} = \frac{2 \cdot 3!}{(n-2)(n-1)n} \frac{1}{c_2 c_1 b} V_{\text{ref}}. \tag{10}$$

The relative quantization error (in LSBs) can also be found. It is given by

$$e_q = \frac{\hat{V}_{\text{in}} - V_{\text{in}}}{V_{\text{LSB}}} = \frac{1}{2} c_2 c_1 b \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k - \frac{1}{2} c_2 c_1 b \frac{(n-2)(n-1)n}{3!} \frac{V_{\text{in}}}{V_{\text{ref}}}. \tag{11}$$

Hence, from (6)

$$V_{i_3}[n] = -2 V_{\text{ref}} e_q \tag{12}$$

as in (3).

Thus, the quantization error can be found in analog form at the output of the last integrator. Note that this derivation is valid only if the digital filter following the modulator is a direct realization of (9) (cf. Section IV).

From (10), the equivalent number of bits (ENOB) can be derived as

$$n_{\text{bit}} = \log_2 \left(\frac{2V_{\text{ref}}}{V_{\text{LSB}}} \right) = \log_2 \left(c_2 c_1 b \frac{(n-2)(n-1)n}{3!} \right) \approx 3 \log_2(n) + \log_2 (c_2 c_1 b) - 2.6 \tag{13}$$

where $n \gg 1$ was assumed.

In design, one needs to find the lowest value of n consistent with the required resolution. Clearly, the resolution increases rapidly with n, but as $b \leq 1$, $c_1 \leq 1$, and $c_2 \leq 1$ hold, it is reduced by an amount dependent on the values of these scale factors. In practice, however, the scale factors cannot be chosen independently, since they affect the stability of the loop. The larger the number of clock periods (n) per conversion cycle is, the smaller the scaling coefficients must be, in order to avoid overloading the integrators. Thus, an optimum choice of n is necessary. It can be achieved by the following steps.

1) Choose the maximum allowable value of the input signal as a fraction of V_{ref}. This is required, as higher order structures will become unstable if the input signal is allowed to approach V_{ref}. In a second-order modulator, e.g., the maximum allowable input is around $0.9V_{\text{ref}}$, while in a third-order one it is less than $0.75V_{\text{ref}}$. However, as the integrators' maximum output, the allowable values of the scaling coefficients (b, c_i), and the required number of cycles n all strongly depend on the maximum input signal, it is sometimes advantageous to limit the input signal even more, so as to reduce n. For example, $0.75V_{\text{ref}}$ or $0.67V_{\text{ref}}$ can be chosen for the second-order converter. For a third-order ADC, even $0.5V_{\text{ref}}$ may be advantageous.
2) Find an initial n_{id} by assuming an unscaled architecture, i.e., $b = c_1 = c_2 = 1$, using (13). (E.g., a 16-bit resolution requires $n_{\text{id}} = 75$ for a third-order loop, while $n_{\text{id}} = 363$ for a second-order one.)
3) Simulate the structure for n_{id} cycles, and get estimates of the scale factors b, c_i from the integrators' maximum output swings.
4) Using the new scale factors, get a new estimate of n using (13).
5) After repeating the previous steps a few (2–3) times, usually neither the coefficients nor n will change significantly. At this point, the smallest allowable number of cycles n has been obtained.

For example, in the design of a third-order modulator with a maximum NTF gain of 1.5, using the Delta-Sigma Toolbox in MATLAB [17], with an input signal reduced to $V_{\text{in}} \leq 0.67V_{\text{ref}}$, the algorithm described above gives $n = 158$ for the optimal number of periods for 16-bit resolution. For a second-order modulator, $n = 537$ clock periods are required.

The derivations can easily be generalized to an arbitrary-order CIFF $\Delta\Sigma$ modulator. The general expression is

$$\frac{V_{\text{in}}}{V_{\text{ref}}} = \frac{1}{\binom{n}{L_a}} \underbrace{\sum_{k_{L_a}=0}^{n-1} \sum_{k_{L_a-1}=0}^{k_{L_a}-1} \cdots \sum_{k_1=0}^{k_2-1}}_{L_a} d_k \tag{14}$$

where L_a is the order of the analog loop.

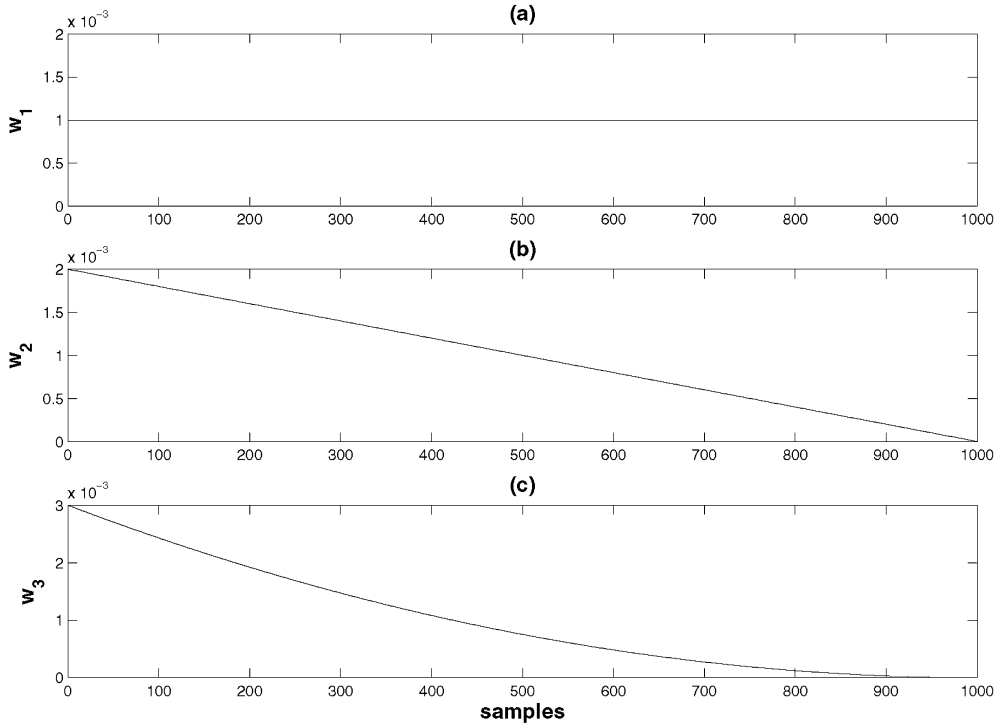


Fig. 5. Weighting functions of *CoI* filters. (a) One integrator. (b) Two integrators. (c) Three integrators.

IV. Digital Filter Design

Although a general formula for calculating the output code was given above in (9), a direct implementation of the formula may not yield the most practical digital filter. Here, optimal design techniques will be discussed for the realization of the digital filter.

A. Direct Calculation of the Digital Output

As discussed in [1] for the first-order incremental converter, and in Section III for higher order ones, the conceptually simplest filter to produce the digital output of the converter is a cascade of integrators implementing the formula given in (9). This results in a filter of the same order as the modulator.

Since the converter operates in an intermittent mode, in the first-order case (assuming one-bit quantization), the filter can be implemented as a simple up-down counter. For higher order filters, only the first stage of the filter can be realized this way, while all other stages must be implemented as digital integrators with adequate register widths. The required precision for the integrators can be calculated as in [18], or optimized by means of simulation.

For a first-order incremental converter, as for the dual-slope one, the output signal is a very close approximation of the average value of $V_{\rm in}$ during the conversion. This means that if $V_{\rm in}$ contains a periodic noise (such as coupled from a power line) with a period T_p, and nT is an integer multiple of T_p (where T is the clock period), then by averaging the output digits of the modulator, the periodic noise can be eliminated. This is a very useful property for converters operating in a noisy environment.

In a higher order structure, the output of the modulator is not simply averaged, but repeatedly accumulated by means of several integrators. As the process is an accumulate-and-dump type realization of the filter and decimator, the final output can be calculated as a weighted sum of the samples in the loop's digital output sequence. Fig. 5 shows the weight factors of three *cascade-of-integrators* (*CoI*) filters. Clearly, for higher order incremental converters, a periodic noise (e.g., line frequency disturbance) is not automatically suppressed using a direct-implementation filter, since the weighting varies asymmetrically from sample to sample.

Note that (as Fig. 5 shows) the digital weighting process places the highest weight on the first few samples. Thus, it is important that the average value of the first few samples of the modulator's output be close to that of the incoming signal. This way, the effects of the transient of the $\Delta\Sigma$ loop will be minimized. This can be achieved by feeding the input signal directly forward to the quantizer (Fig. 4), assuring that the first output signal samples will already give a valid representation of the input signal.

The *CoI* scheme does not provide suppression of periodic noise (usually line-frequency noise) affecting the converter. Such suppression may be obtained by including an S/H stage at the input of the loop, operating at twice the noise frequency, and averaging two consecutive outputs. In some applications involving control loops, multiplexed inputs, etc. an S/H stage may be needed anyway.

As will be shown in Section IV-C, by using a different design approach, it is possible to suppress periodic noise in higher order incremental converters.

Fig. 6 shows a second-order incremental converter with a second-order output filter. Fig. 7(a) shows the quantization error calculated from the output of the second *digital* integrator (with 10-bit resolution), while Fig. 7(b) shows the output of the second *analog* integrator (at the end of the conversion).

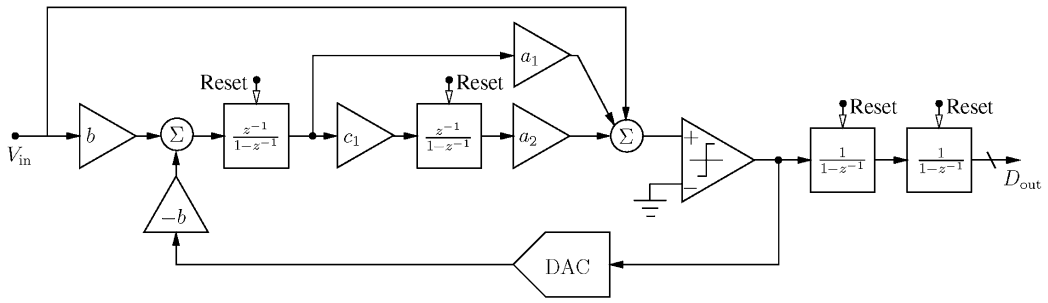


Fig. 6. Second-order incremental converter with second-order digital filter.

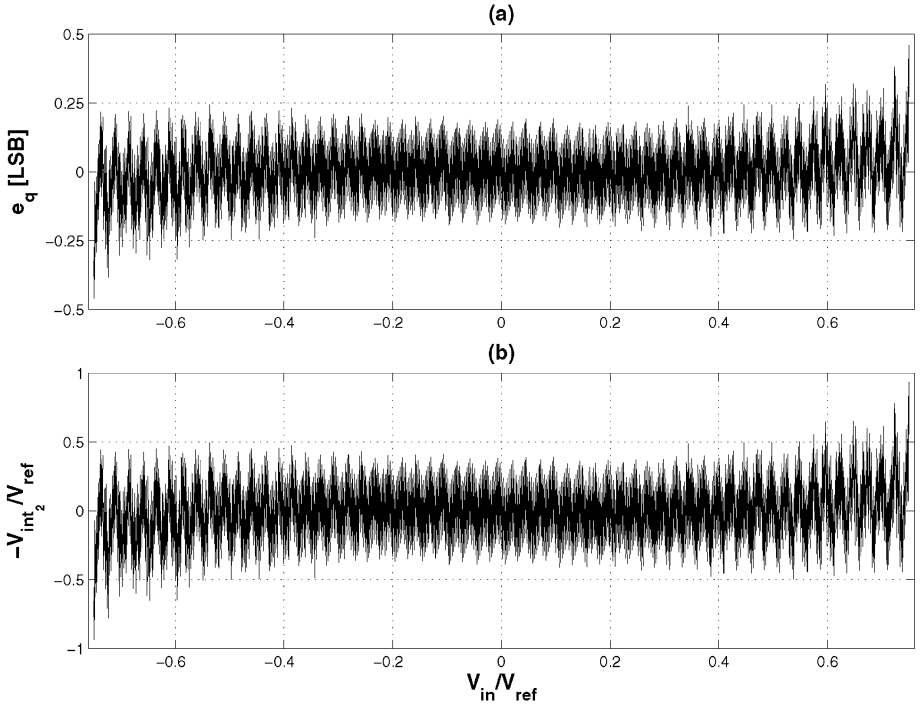


Fig. 7. Simulation result of a second-order system with 10-bit resolution. (a) Quantization error. (b) Output of the second integrator (inverted).

The simulation result shows a good agreement with (12). Hence, the output signal of the last integrator can be used to improve the accuracy of the digital output word by feeding it to another A/D converter (either to an additional one or to the same converter, as in [8]). In the simplest case, one can detect the sign of the output of the last integrator and use it to gain an extra bit. Using such manipulations, the required number of cycles can be further reduced.

B. Higher Order Filtering With Dither

Section IV-A and the equations derived above suggest that filtering an L_ath-order modulator with L_ath-order digital filter yields the most accurate output, and the speed/resolution tradeoff cannot be further improved. It was also stated in [4] that using a higher order (say $L_a + 1$st-order) filter the resolution and the average accuracy may be increased, but the quantization error around zero remained the same [4, Fig. 6]. Fig. 8(a) shows the quantization error of a first-order incremental converter with first-order filtering, while Fig. 8(b) shows the quantization error of the same converter with a second-order filter (using two digital integrators at the output).

The unchanged peak error can be explained by realizing that for a very small dc input signal, the linearized models of the quantizer and the modulator are no longer valid. Instead, the actual operation needs to be analyzed in the time domain. Consider the first-order incremental converter [Fig. 1(a)]. Comparing Fig. 8(a) and (b), one can see that for the second-order filter, the anomaly arises when the input signal is within ± 0.5 LSB. Recalling the operation of the first-order incremental converter (Fig. 1(b)), it is clear that when the incoming signal is this small, it does not trigger a transition of the comparator during the limited number of cycles (n). Hence, no feedback is applied, and the loop does not become functional. Note that in a $\Delta\Sigma$ converter, similar "dead-zones" exist around other input values (typically around low-order fractions of V_{ref}); in this case, the transition of the comparator is triggered at those inputs; thus, the effect is most significant around zero.

This "dead-zone" problem can be eliminated, and hence the higher order filter becomes effective, if the comparator is forced to make decisions and thus the whole loop is forced to operate even for extremely small input signals. This can be achieved by dithering. Injecting a dither signal into the loop right before

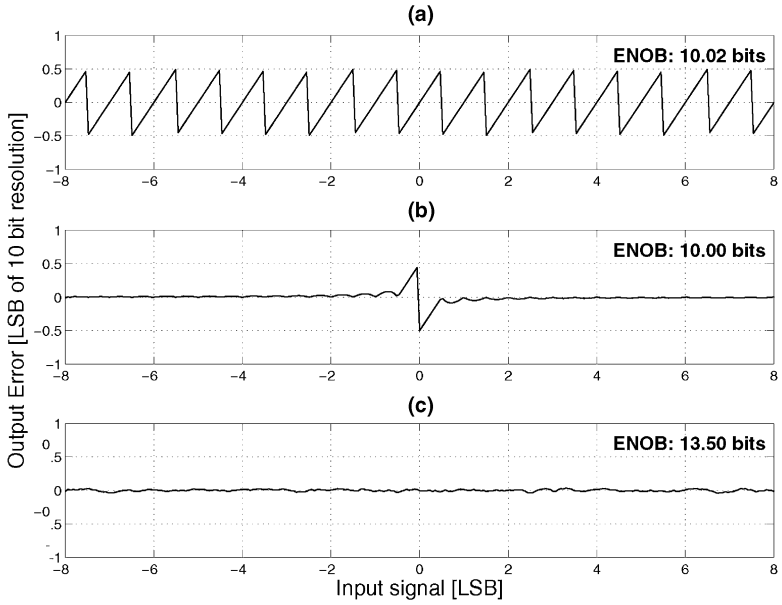


Fig. 8. Quantization error of a 10-bit first-order converter around zero input. (a) Using first-order digital filter. (b) Using second-order digital filter (two integrators). (c) Using second-order filter with dither signal injected into the loop.

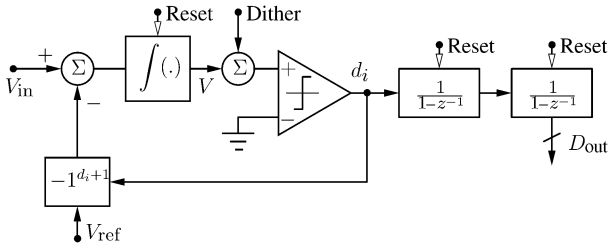


Fig. 9. Improved first-order converter with second-order filtering and dither.

the quantizer [3, Ch.3] (Fig. 9) can eliminate the error peaks around zero. This solution has several advantages: the dither signal is shaped by the NTF the same way as the quantization error is, so it is high-pass filtered, and hence should not affect the measurement of the dc signal significantly.

Due to the transient operation of the converter, the average value of the dither signal divided by n (the number of cycles) may increase the variance of the output digital samples. This error can be reduced below 0.5 LSB by properly setting the variance of the dither and the number of cycles. Alternatively, if the dither signal is a zero-mean pseudorandom signal of length n generated digitally, it can be repeated periodically with a period of n clock cycles. This will eliminate this added error completely.

For effective dithering, the amplitude needed for the injected dither signal should be fairly large (typically 0.3–0.6 LSB of the quantizer). Although the dither is shaped by the NTF, it causes a few decibels reduction in the permissible input signal range, and hence in the dynamic range. It can be shown that if the dither is k times smaller then the LSB of the quantizer, then (applying the linear model) the dynamic range reduction D_r in decibels is

$$D_r = 10 \log \left(1 + \frac{1}{k^2}\right). \tag{15}$$

For example, if $k = 2$ (the dither is 0.5 LSB), then, the reduction in the dynamic range is $D_r = 0.97$ dB, or 0.16 bits.

To verify the effectiveness of this technique, a 10-bit first-order converter (Fig. 9) was simulated by means of MATLAB. The filtered quantization errors are shown in Fig. 8 for various digital filters and dither conditions. In the first case [Fig. 8(a)], the filter is a simple counter, and the error of the output signal is similar to that of a Nyquist-rate converter. Fig. 8(b) shows the output of the same converter, but using a second-order digital filter. Even though the resolution is increased overall, the accuracy around zero remained the same. Applying uniform dither signal in the loop with a maximum value equal to 0.5 LSB of the quantizer in the loop, the large error around zero input was eliminated. The resolution of the converter with the same length of operation (n) was increased by 3.5 bits (21 dB), without modifying the analog hardware significantly. Thus, while a first-order converter with a first-order digital filter requires $n = 2^{13} = 8192$ cycles to get 13-bits resolution, the same converter using second-order filtering with dither can deliver the same performance with less than $2^{10} = 1024$ cycles.

For higher order loops, the *CoI* scheme which is based on simple time-domain considerations and ignores the spectral distribution of the quantization noise, is not effective. Then, the "running-average" or "sinc" filters, highly popular among $\Delta\Sigma$ ADC designers, are preferable. They can also provide periodic noise suppression. Their operation and design is discussed in Section V.

C. Filtering Using Sinc^L Filters

As discussed in Sections IV-A and B [cf. Fig. 5], if an asymmetric weighting function is used, there is no suppression of a periodic disturbing signal. However, using a symmetrical weighting function, it is possible to suppress noise occuring at line frequency and other periodic noises. The techniques discussed below can be used for first-order as well as higher order converters.

A symmetrical weighting function and its realization were proposed in [19]. An efficient implementation, using a cascade of integrators and differentiators, was introduced in [18]. It can be optimized for $\Delta\Sigma$ modulators [3], [20]. This so-called "sinc-filter" is a very effective and popular structure for $\Delta\Sigma$ decimator design. In this subsection the specific filter design considerations for incremental converters are focused on.

An Lth-order sinc-filter with a decimation ratio of M has the finite-impulse response (FIR) transfer function

$$H(z) = \frac{1}{M^L}\left(1 + z^{-1} + \cdots + z^{-M+1}\right)^L = \frac{1}{M^L}\left(\frac{1 - z^{-M}}{1 - z^{-1}}\right)^L \tag{16}$$

where $z = e^{sT}$, and $T = 1/f_s$. The filter is characterized by two parameters. The first one is the order of the filter (L), and the second is the decimation ratio (M). The filter has zeros at frequencies kf_s/M, $k = 1, 2, \ldots, M-1$. The first notch f_1 occurs at f_s/M, and hence this frequency can be considered the edge of the stopband of the filter. If the output of the filter is decimated by M, the noise which folds down to dc will be centered around f_1 and its integer multiples, and hence will get suppressed by the notches of the filter response.

In the case of the incremental converter, the order of the filter needs to be at least as high as that of the modulator, and preferably higher by 1, as can be seen from the derivations of Section III. However, the decimation ratio M of the filter needs to be determined differently from that of a conventional $\Delta\Sigma$ modulator. As for the $\Delta\Sigma$ loop, the resolution of the incremental converter loop improves with increased M. However, other considerations also apply. Usually, the first notch frequency, located at $f_1 = f_s/M$, is used to suppress the noise at the line frequency f_l, so it is fixed. This leaves f_s as the variable to determine. There is a tradeoff: if f_s is chosen too large, M will also be large, and—as will be shown in the following—the number of clock periods needed for the measurement is unnecessarily extended. Also, the power and chip area requirements of the opamps in the analog loop will be higher than necessary. If, on the other hand, f_s is made too low, the quantization noise will not be adequately suppressed by the loop, and also the thermal noise effects will require overly large input capacitors in the switched-capacitor implementation of the analog feedback loop.

Since the incremental converter always operates in a transient mode, the transients of both the analog and digital component blocks must settle sufficiently to achieve the specified accuracy. For the analog loop, the settling condition was given in (13). For the FIR digital filter, the concern is that all memory elements must be filled with valid data to get a correct digital output.

The total "length" of the FIR filter (i.e., the number of samples in its impulse response) is $LM - (L-1)$, as can be seen from (16). If the filter is realized using the structure of [18], the length is somewhat greater, LM. Thus, to fill all registers, the converter and the filter must be operated for at least LM clock cycles.

Thus, there are two constraints on the minimum number of clock periods n during which the converter must be operated to achieve a specified resolution n_{bit}. One is (13) which gives the relation between n_{bit} and n for the analog loop alone, and the other is the relation $n \geq LM$ derived above. For higher order filters, the latter condition usually leads to a higher required value, and hence it determines $n_{\min}$.

To fulfill all the above requirements, the following "cookbook" procedure is suggested.

1) Choose the analog modulator order $(L_a = 2, 3, \ldots)$.
2) This determines the order of the sinc filter $(L = L_a + 1)$.
3) Find $n_{\min} = n$, the required number of cycles using (13) and the iterative procedure described there; increase $n_{\min}$ until L becomes its divider.
4) Let $M = n_{\min}/L$.
5) Simulate the whole system and check the achievable resolution.
6) If the required n_{bit} resolution is not achieved, increase $n_{\min}$ with L.
7) Repeat the last two steps until the desired resolution is achieved.
8) When $n_{\min}$ and thus M is found, the clock frequency can be calculated as $f_s = Mf_l$, where f_l is the line frequency.

Note that with the increase of $n_{\min}$, the scaling coefficients also have to be updated to prevent the overflow of the analog integrators. However, in practice, the algorithm is not too sensitive, and with a few iteration steps, one can get good parameters for a given resolution.

Also, it should be noted that the described algorithm did not take into account the presence of thermal noise, which depends on the sampling frequency and the capacitor values of the modulator. If the size of the capacitors becomes too large with the f_s derived from the noiseless case above, then, f_s must be increased until the desired SNR is achieved. In this case, the resolution limiting factor will be not the quantization error but the thermal noise.

As an example for the ideal model, $n_{\min} = 537$ is required for a second-order modulator with $u_{\max} = 0.66V_{\text{ref}}$ and 16-bit resolution. Using only a second-order sinc-filter, the required number of cycles for the same resolution becomes 1092, showing the ineffectiveness of this structure. However, using a third-order sinc-filter, the required number of cycles drops to $n = 576$, which is only slightly larger then the ideal one, while at the same time it has the useful property of periodic noise suppression. In the case of a third-order modulator with a fourth-order filter, 16-bit resolution requires $n = 352$ cycles. A detailed comparison between the different design choices is given in Section VI.

D. Line-Frequency Noise Suppression

Converters designed for high-accuracy dc measurement often require a suppression of the line frequency ($f_l = 50$ Hz or 60 Hz). For dual-slope converters, this can be achieved by setting the time interval of the incoming signal's integration to be an integer multiple of $1/f_l$.

As discussed above, sinc-filters can also be designed to provide line-frequency noise suppression. To achieve this, one of

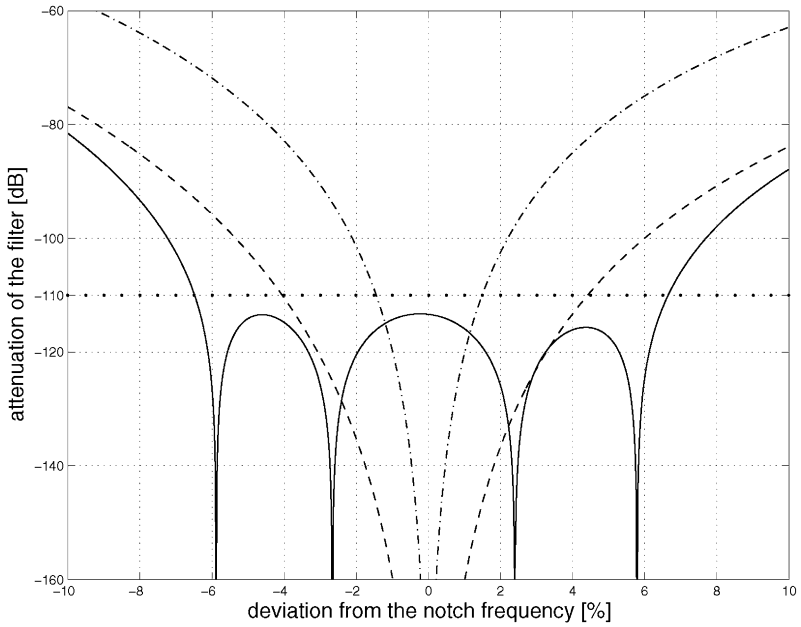


Fig. 10. Transfer function of different filters around the line frequency: third-order sinc-filter (dash-dot line), fourth-order sinc-filter (dashed line), and fourth-order filter with staggered zeros (solid line).

the notches of the filter must coincide with the line frequency f_l. This gives the condition

$$f_s = M\frac{f_l}{k} = \frac{nf_l}{Lk}, \qquad k = 1, 2, \ldots, M-1. \tag{17}$$

Here, the condition $n = ML$ (derived earlier) was used.

To make the gain response as flat as possible at low frequencies, and also to obtain a reasonably high sampling rate for the analog portion of the circuit to reduce inband thermal noise, normally $k = 1$ is chosen in (17).

Note that (as discussed in Section IV-B) a good choice for the order L of the digital filter is $L_a + 1$, where L_a is the order of the analog loop filter.

In critical applications, the suppression available by using straight sinc-filters may not be adequate, especially if the line frequency and/or the on-chip oscillator frequency is inaccurate. In this case, the zeros of the sinc-filter can be staggered around f_l, thus widening the frequency range where the rejection is high.

To modify the zeros of the filter, the rotated sinc (RS) filter introduced by Lo Presti [21] may be used. A second-order factor of its transfer function is of the form

$$H_{\rm dec}(z) = \frac{1 - 2(\cos M\alpha)z^{-M} + z^{-2M}}{1 - 2(\cos\alpha)z^{-1} + z^{-2}} \tag{18}$$

where $z = e^{j2\pi f/f_s}$, and α represents the angle of the modified complex conjugate zeros. If $\alpha = 0$, the expression simplifies to the transfer function of a second-order classical sinc filter.

If a required suppression is given in a region (say $f_l \pm 5\%$), one can optimize the order of the sinc filter and the number of RS second-order filter blocks to achieve the given suppression [21].

Since the required frequency range is usually small compared to the line frequency, α is usually also small. Thus, $2(\cos N\alpha)$ and $2(\cos\alpha)$ can be implemented as $2 - n_1$ and $2 - d_1$, respectively. Here, the small quantities n_1 and d_1 can be chosen as negative powers of 2. It can be also shown that $n_1 = M^2 d_1$. A detailed discussion of this technique can be found in [22].

As $n_1 = M^2 d_1$, in cases when M is high (say $M = 256$), the required register-width may become excessive. In these cases, two-stage decimation may reduce the required precision. The first stage can have a high oversampling ratio (e.g., $M_1 = 32$) and can be implemented with a straight fourth-order structure. The second stage, which implements the staggered zeros, should have a lower oversampling ratio (e.g., $M_2 = 8$), such that $M_1 M_2 = M$. With such low M_2, the coefficients n_i and d_i are much easier to implement.

Fig. 10 compares the achievable rejection around the line-frequency achieved using various filter configurations. If the required attenuation of the line frequency is -110 dB, then, the third-order, fourth-order, and modified fourth-order filter can obtain this attenuation in the ranges $f_l \pm 1.5\%$, $f_l \pm 4\%$, and $f_l \pm 6.5\%$, respectively.

A similar technique can be used to suppress both $f_l = 50$ Hz and $f_l = 60$ Hz simultaneously using the same clock frequency.

E. Effect of Gaussian Input Noise Added to a DC Input Signal

It is also interesting to study the converter output when the input signal is the sum of a dc signal and gaussian noise with zero mean and σ_g^2 variance.

If the modulator contains a feedforward input path, i.e., the input signal is fed to the input of the quantizer (Fig. 4), then, the output of the modulator is

$$y[k] = u_{\rm dc} + n_g[k] + e_q[k] * h[k] \tag{19}$$

where $u_{\rm dc}$ is the applied dc input signal, $n_g[k]$ is the Gaussian input noise, $h[k]$ is the inverse z-transform of the NTF, and $e_q[k] * h[k]$ is the output quantization error. Thus, in this architecture, the input signal appears in the output without being modified or delayed [23].

After n cycles, the output samples weighted by the digital filter are summed. Theoretically, if the output of the modulator contained only the dc signal and the Gaussian noise, and the weights of the filter were equal ($w_i = 1/n$, i.e., simple averaging), then, the variance of the output signal would become σ_g^2/n. This is the best linear unbiased estimator for the mean value of the input signal based on n samples.

However, using higher order filtering, the weighting coefficients of the filter are not equal, and thus the variance of the output signal becomes

$$\sigma_y^2 = n\sum_{i=1}^{n} w_i^2\sigma_g^2 > \frac{\sigma_g^2}{n}. \tag{20}$$

Note that $\sum_{i=1}^{n} w_i = 1$ is always satisfied, provided that the transfer function of the filter is equal to 1 at dc. With this condition, it can be shown that

$$n\sum_{i=1}^{n} w_i^2 \le \frac{4}{3} \approx 1.33 \tag{21}$$

for second-order *CoI* filters and

$$n\sum_{i=1}^{n} w_i^2 \le \frac{9}{5} = 1.8 \tag{22}$$

for third-order *CoI* filters.

Hence, although the converter does not optimally average the noise, the output variance satisfies

$$\sigma_y^2 < 2\frac{\sigma_g^2}{n} \tag{23}$$

indicating a reasonably good noise suppression.

Note that the above discussion did not take into account the quantization noise also present in the output. However, the quantization noise after the filtering can be modeled as an additive uniform noise with a variance $V_{\mathrm{LSB}}^2/12$. Thus, the incoming noise must be significantly larger than the quantization error to affect the output. Hence, its variance needs to satisfy

$$\frac{\sigma_g^2}{n} \gg \frac{V_{\mathrm{LSB}}^2}{12}. \tag{24}$$

Simulations of a second-order system with 10- and 15-bit resolutions (corresponding to $n = 60$ and $n = 378$, respectively) agreed well with the theory discussed above. In the first case, using an input noise with a variance $\sigma_g > 4V_{\mathrm{LSB}}$ started to show up in the output as a disturbing signal. In the second case, $\sigma_g > 8V_{\mathrm{LSB}}$ caused a similar effect. The variances were comparable to those predicted by the equations above.

V. Circuit-Level Considerations

In Sections II–IV, the theoretical operation of the incremental converter was discussed. In practice, however, nonideal effects are expected to degenerate the performance of the converter, and must be considered in the design process. Those topics which are different from a regular $\Delta\Sigma$ modulator design will be discussed in this Section. More details can be found in, e.g., [3], [24], [25].

A. Design Techniques

To design the loop, the well-known methods available for $\Delta\Sigma$ modulators can be used [3, Ch. 4–5], [17]. However, due to the special properties of the incremental converter, some additional considerations must be observed. As the converter is primarily used for dc signals, proper scaling of the coefficients is required to prevent the overflow of the integrators. This can be done by means of simulation, as discussed earlier in this paper (cf. Section III).

In $\Delta\Sigma$ design, it is usually preferable to spread the zeros of the NTF across the pass band [3, Sec. 4.4]. However, this method should not be used in incremental converters, as the main goal is to provide the most noise suppression at dc.

The linearity requirements for the components used in incremental converters are usually quite severe. Capacitor nonlinearity will be discussed later. Opamp nonlinearity can also degenerate the performance. To reduce this, a low-distortion architecture can be used [23], which contains a feedforward path for the input signal directly to the quantizer. As a result, the input signal is not processed by the analog integrators, and hence the effects of opamp nonlinearities are greatly reduced.

B. Offset and Asymmetry Errors

Since the circuit is intended for dc inputs, offset errors must be kept very small, within an LSB. In addition, charge-injection caused by the nonideal switches needs to be made signal-independent by properly delaying the operation of floating switches in the modulator [24, Ch.10]. Correlated double sampling may be used in the first stage of the analog modulator to reduce its offset [24, Ch.10], [25]. Also, asymmetry in the upper and lower halves of the differential circuit can introduce errors.

Both offset and asymmetry errors can be reduced by using a correction scheme in which the conversion by the $\Delta\Sigma$ loop is performed in two cycles: once with normal inputs, and then with inverted polarity [1]. During the second cycle, the output of the comparator is also complemented. The two output sequences thus obtained can then be added (with the first sequence delayed by $NT/2$), and the offset and asymmetry errors will be cancelled. This scheme was used in [1] for a first-order loop, and can be adapted for modulators of any order. This method can be easily implemented, as the converter operates in transient mode.

C. Capacitor Nonlinearity

If a high resolution (20 bits or more) is required, it is possible that the linearity of the capacitors available with a given technology cannot satisfy the linearity requirements for the given resolution. In this case, simple circuit techniques may be used to alleviate the resulting nonlinear conversion errors. It is possible, e.g., to combine two capacitors with opposite polarities in parallel and/or in series to obtain a first-order cancellation of the nonlinear errors.

If such measures are not sufficient to reduce the distortion to acceptable levels, consideration may be given to using multibit internal quantization in the $\Delta\Sigma$ loop, as described in Section V-D. This will reduce the voltage swing across the input capacitors, and thus reduce the distortion.

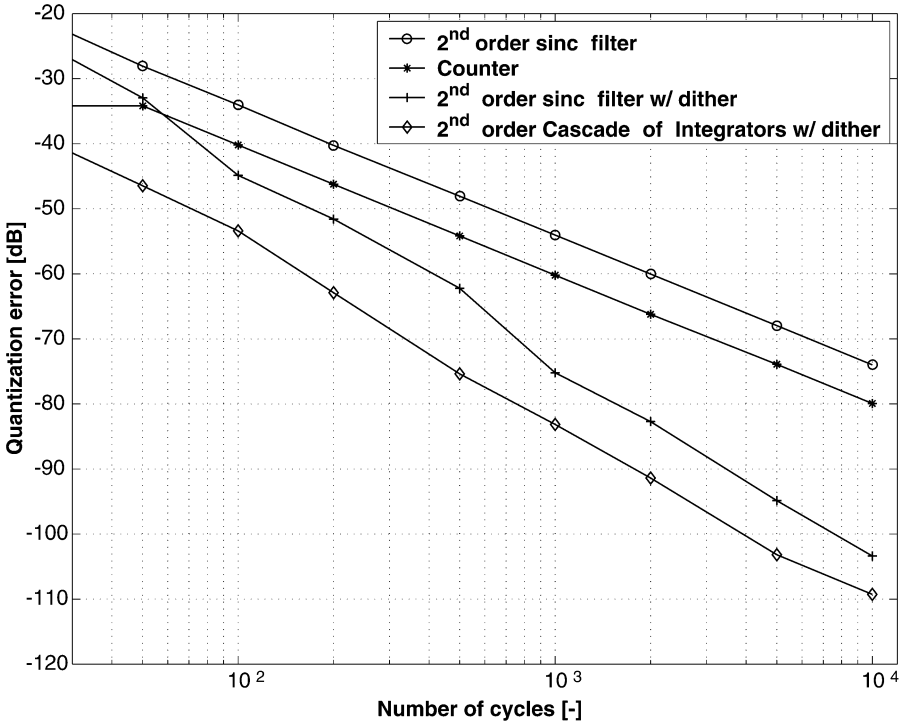


Fig. 11. Quantization error as a function of the number of cycles, with different filter configurations for a first-order converter loop.

D. Multibit Quantization

If multibit quantization is used in the loop, the feedback digital–analog converter (DAC) will introduce gain and linearity errors. However, the gain error can be eliminated using a two-point calibration of the converter, and the inband mismatch error can be made negligible by using a unit-element DAC incorporating a dynamic element matching process such as data weighted averaging (DWA) [26]. DWA rotates the usage of the elements, greatly reducing the inband mismatch error, if it is combined with dithering.

As the incremental converter works in transient mode, the elimination of inband errors will not be perfect. However, it can be easily shown that the residual error due to mismatch is bounded by

$$\epsilon \leq \frac{\frac{N}{2}\epsilon_m}{n} \tag{25}$$

where ϵ_m is the rms mismatch error of the elements of the DAC ($\sim$0.1–1%), N is the number of unit elements and n is the number of clock cycles during which the converter operates. Using multibit feedback, the required number of cycles can be significantly reduced, thus improving the conversion speed.

VI. Examples

In this section, different converters satisfying similar specifications are compared. In general, these may be designed to achieve one of two different goals.

1) If only moderate resolution is needed, and the main requirement is to minimize the chip area and/or the power consumption, then a first-order incremental converter is usually optimal. Depending on other requirements (such as suppression of line-frequency noise, high-speed operation, etc.), different digital filter configurations may be used. This issue is discussed below in Section VI-A.
2) If the main goal is to achieve high resolution as well as high speed, higher order converters will be required. Again, there are several possibilities, depending on the other requirements. High-order converter design examples are discussed below in Section VI-B.

A. First-Order Converters

As mentioned above, first-order incremental converters can be used with different filters. Fig. 11 compares the quantization errors in decibels as a function of the number of cycles for a variety of applicable digital filters. It can be seen that applying a second-order sinc filter to the output of an undithered $\Delta\Sigma$ modulator gives the largest error among the filters evaluated, while a second-order *CoI* digital filter cascaded with a dithered loop gives the best resolution. A simple counter, such as the one described in [1], gives an intermediate result.

In obtaining the results displayed in Fig. 11 and in Tables I and II, the iterative optimization technique (Steps 1 to 5) discussed at the end of Section III was used. Nonidealities such as kT/C noise were ignored, and may require longer operation than the results given here suggest.

Tables I and II compare the performance of the same filters for specified resolution and for specified number of operational cycles, respectively. Specifically, in Table I the required numbers of samples are shown for 10-bit resolution. As already stated, the second-order *CoI* filter with dither signal gives by far the lowest required number of cycles. However, this design solution needs additional hardware to implement the dither signal, and the system cannot suppress incoming periodic noise.

TABLE I
COMPARISON OF FIRST-ORDER INCREMENTAL CONVERTERS I

Type of Digital Filter	Resolution (Accuracy)	Number of Cycles
second-order sinc	10 bit	2500
1 integrator (counter)	10 bit	1024
second-order sinc with dither	10 bit	500
2 integrators with dither	10 bit	180

TABLE II
COMPARISON OF FIRST-ORDER INCREMENTAL CONVERTERS II

Type of Digital Filter	Resolution (Accuracy)	Number of Cycles
second-order sinc	8.6 bit	1024
1 integrator (counter)	10.0 bit	1024
second-order sinc with dither	12.2 bit	1024
2 integrators with dither	13.5 bit	1024

Table II shows the achievable resolution if the number of cycles is limited to 1024. Again, the best resolution can be achieved by the *CoI* configuration following a dithered loop.

In conclusion, if in a given design situation the most important factor is the smallest possible chip area, then a first-order incremental converter with a counter may give the optimum solution. If, on the other hand, chip area, power consumption and speed are all factors to be considered, a first-order converter with a second-order *CoI* filtering and dither can be the solution.

B. Higher Order Converters

Table III lists the coefficients of the optimized second- and third-order modulators which were used to evaluate the different configurations throughout this section (a maximum input signal $V_{\text{in,max}} = 0.67V_{\text{ref}}$ was assumed). The notations used for the coefficients follow Fig. 4. They were optimized by means of the iterative algorithm described at the end of Section III.

TABLE III
COEFFICIENTS OF SIMULATED MODULATORS

Mod. order	Filter Type	a_1	a_2	a_3	c_1	c_2	b
2	2 integrators	1.72	1.03	N/A	0.64	N/A	0.72
2	third-order sinc	1.72	1.08	N/A	0.61	N/A	0.72
3	3 integrators	1.26	0.81	0.43	0.56	0.29	0.63
3	fourth-order sinc	1.26	0.81	0.43	0.56	0.29	0.63

Table IV compares the performance of various higher order modulators with a variety of filters. The assumed resolution is 16 bits, and the total number of cycles required is tabulated.

TABLE IV
COMPARISON OF HIGHER ORDER INCREMENTAL CONVERTERS

Order of Modulator	Type of Digital Filter	Resolution (Accuracy)	Total Number of Cycles
2	2 integrators	16	537
2	2 integrators†	16	381
2	second-order sinc	16	1092
2	third-order sinc	16	576
3	3 integrators	16	158
3	3 integrators†	16	127
3	fourth-order sinc	16	350

†With the sign of the loop filter output used to gain an extra bit of resolution.

As for the first-order converter, the fastest settling time was obtained by combining a loop with a *CoI* filter of the same order as that of the loop and detecting the sign of the output of the last integrator to pick up an extra bit. However, if effective suppression of line-frequency noise is required, then, combining an Lth-order modulator with an $L+1$st-order sinc filter may be a preferable choice. Note that the coefficients of the second-order modulator change rapidly with changing n, while those of the third-order hardly change even if n is doubled.

VII. CONCLUSION

In this paper, theoretical analysis and design methods were described for first- and higher order incremental converters. A general method of calculating the digital output signal of the modulator loop was described in Section III, and used to derive a lower bound for the number of samples required for a specified accuracy.

It was shown for the special case of a first-order converter that the speed/resolution tradeoff can be significantly improved by injecting a dither signal into the loop, and by applying higher order digital filtering. Comparisons between different filter configurations showed that although the most area-efficient converter is a combination of a first-order modulator with a counter-type filter realization, in high-resolution applications the use of higher order filtering combined with dithering in the loop may enhance the speed and reduce power consumption significantly.

For higher order loops, the choice of the optimal filter depends on the application and the specification of the converter. When line-frequency noise suppression is required, a sinc filter may provide the optimum solution. However, if settling time, speed, digital circuit complexity and power consumption all need to be optimized, a *CoI* filter may represent a better tradeoff.

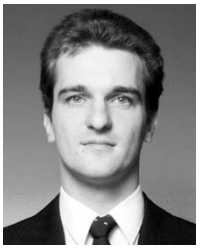
ACKNOWLEDGMENT

The authors would like to thank Prof. I. Kollár for his useful comments.

REFERENCES

[1] J. Robert, G. C. Temes, V. Valencic, R. Dessoulavy, and P. Deval, "A 16-bit low-voltage A/D converter," *IEEE J. Solid-State Circuits*, vol. 22, pp. 157–163, Apr. 1987.

[2] R. van de Plassche, *Integrated Analog-to-Digital and Digital-to-Analog Converters*. London, U.K.: Kluwer Academic, 1994.
[3] S. R. Norsworthy, R. Schreier, and G. C. Temes, Eds., *Delta–Sigma Data Converters*. Piscataway, NJ: IEEE Press, 1997.
[4] J. Robert and P. Deval, "A second-order high-resolution incremental A/D converter with offset and charge injection compensation," *IEEE J. Solid-State Circuits*, vol. 23, pp. 736–741, June 1988.
[5] O. J. A. P. Nys and E. Dijkstra, "On configurable oversampled A/D converters," *IEEE J. Solid-State Circuits*, vol. 28, pp. 736–742, July 1993.
[6] R. Harjani and T. A. Lee, "FRC: A method for extending the resolution of nyquist rate coverters using oversampling," *IEEE Trans. Circuits Syst. II*, vol. 45, pp. 482–494, Apr. 1998.
[7] C. Jansson, "A high-resolution, compact, and low-power ADC suitable for array implementation in standard CMOS," *IEEE Trans. Circuits Syst. I*, vol. 42, pp. 904–912, Nov. 1995.
[8] P. Rombouts, W. de Wukde, and L. Weyten, "A 13.5-b 1.2-V micropower extended counting A/D converter," *IEEE J. Solid-State Circuits*, vol. 36, pp. 176–183, Feb. 2001.
[9] G. Mulliken, F. Adil, G. Cauwenberghs, and R. Genov, "Delta-sigma algorithmic analog-to-digital conversion," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 4, Scottsdale, AZ, May 26–29, 2002, pp. 687–690.
[10] (2003) AD77xx Product Family Datasheets. Analog Devices, Norwood, MA. [Online]. Available: http://www.analog.com
[11] (2003) ADS124x Product Family Datasheets. Burr-Brown (Texas Instruments), Dallas, TX. [Online]. Available: http://www.ti.com/
[12] (2003) CS55xx Product Family Datasheets. Cirrus Logic, Austin, TX. [Online]. Available: http://www.cirrus.com
[13] (2003) LTC24xx Product Family Datasheets. Linear Technology, San Jose, CA. [Online]. Available: http://www.linear.com
[14] J. Johnston, "New design techniques yield low power, high resolution delta–sigma and SAR ADCs for process control, medical, seismic and battery-powered applications," in *Proc. 1st Int. Conf. Analogue to Digital and Digital to Analogue Conversion*, Swansea, U.K., 1991, pp. 118–123.
[15] C. Lyden, "Single shot Sigma Delta analog to digital converter," U.S. Patent 5 189 419, Feb. 23, 1993.
[16] C. Lyden, C. A. Ugarte, J. Kornblum, and F. M. Yung, "A single shot sigma–delta analog-to-digital converter for multiplexed applications," in *Proc. IEEE Custom Integrated Circuits Conf.*, Santa Clara, CA, May 1–4, 1995, pp. 203–206.
[17] R. Schreier. (2003) The Delta–Sigma toolbox v6.0 (Delsig). Mathworks, Natick, MA. [Online]. Available: http://www.mathworks.com/matlabcentral/fileexchange/
[18] E. B. Hogenauer, "An economical class of digital filters for decimation and interpolation," *IEEE Trans. Acoust., Speech Signal Processing*, vol. 29, pp. 155–162, Apr. 1981.
[19] J. C. Candy, Y. C. Ching, and D. S. Alexander, "Using triangularly weighted interpolation to get 13-bit PCM from a sigma–delta modulator," *IEEE Trans. Comm.*, vol. 24, pp. 1268–1275, Nov. 1976.
[20] J. C. Candy, "Decimation for sigma–delta modulation," *IEEE Trans. Comm.*, vol. 34, pp. 72–76, Jan. 1986.
[21] L. Lo Presti, "Efficient modified-sinc filters for sigma–delta A/D converters," *IEEE Trans. Circuits Syst.*, vol. 47, pp. 1204–1213, Nov. 2000.
[22] L. Lo Presti and A. Akhdar, "Efficient antialiasing decimation filter for $\Delta\Sigma$ converters," in *Proc. 5th IEEE Int. Conf. Electronics, Circuits, and Systems*, vol. 1, Lisbon, Portugal, Sept. 7-10, 1998, pp. 367–370.
[23] J. Silva, U.-K. Moon, J. Steensgaard, and G. C. Temes, "A wideband low-distortion delta–sigma ADC topology," *Electron. Lett.*, vol. 37, no. 12, pp. 737–738, 2001.
[24] D. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: Wiley, 1997.
[25] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, pp. 1584–1614, Nov. 1996.
[26] R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit delta–sigma A/D and D/A converters using data weighted averaging," *IEEE Trans. Circuits Syst. II*, vol. 42, pp. 753–762, Dec. 1995.



János Márkus (S'02) received the M.S. degree in electrical engineering in 1999, from the Budapest University of Technology and Economics (BUTE), Budapest, Hungary, where he is currently working toward the Ph.D. degree in the Department of Measurement and Information Systems

In 2000, he was a Design Engineer at Panda Audio Ltd. (a subsidiary of Akai Professional), Budapest, Hungary. In 2001 and 2002, he was an exchange visitor at Oregon State University, Corvallis, OR, in the Department of the Electrical and Computer Engineering. His current research interests include quantization errors in digital signal-processing systems, analog–digital and digital–analog converter testing and Delta–Sigma converter structures.

José Silva (S'98) received the graduate degree in electrical and computer engineering from the Instituto Superior Técnico (IST), Lisbon, Portugal, in 1994. Since September 1997, he has been working toward the Ph.D. degree at Oregon State University, Corvallis, OR.

In 1993, he joined the Integrated Circuits and Systems Group, IST. In 1996 and 1997, he was a Design Engineer at Landis & Gyr (now Siemens Metering), Zug, Switzerland. His current research interests include delta–sigma signal processing and high-speed switched-capacitor circuits.

Gabor C. Temes (SM'66–F'73–LF'98) received the undergraduate degree from the Eötvös University, Budapest, Hungary, in 1956, the Ph.D. degree in electrical engineering from the University of Ottawa, Ottawa, ON, Canada, in 1961, and an honorary doctorate from the Technical University of Budapest, Budapest, Hungary, in 1991.

He held academic positions at the Technical University of Budapest, Stanford University, Stanford, CA, and the University of California at Los Angeles (UCLA). He worked in industry at Northern Electric R&D Laboratories (now Bell-Northern Research), Ottawa, Canada, as well as at Ampex Corp. He is now Professor in the Department of Electrical and Computer Engineering at Oregon State University (OSU). He served as Department Head at both UCLA and OSU. His recent research has dealt with CMOS analog integrated circuits, as well as data converters and integrated sensor interfaces. He is co-editor and coauthor of *Modern Filter Theory and Design* (NewYork: Wiley, 1973); coauthor of *Introduction to Circuit Synthesis and Design* (NewYork: McGraw-Hill, 1977); coauthor of *Analog MOS Integrated Circuits for Signal Processing* (NewYork: Wiley, 1986); co-editor and coauthor of *Oversampling Delta–Sigma Data Converters* (NewYork: IEEE Press, 1992) and of *Delta–Sigma Data Converters* (Piscataway,NJ: IEEE Press, 1997), as well as a contributor to several other edited volumes. He has published approximately 300 papers in engineering journals and conference proceedings.

Dr. Temes was an Associate Editor of the *Journal of the Franklin Institute*, Editor of the IEEE TRANSACTIONS ON CIRCUIT THEORY and Vice President of the IEEE Circuits and Systems (CAS) Society. In 1968 and in 1981, he was co-winner of the CAS Darlington Award, and in 1984 winner of the Centennial Medal of the IEEE. He received the Andrew Chi Prize Award of the IEEE Instrumentation and Measurement Society in 1985, the Education Award of the IEEE CAS Society in 1987, and the Technical Achievement Award of the IEEE CAS Society in 1989. He received the IEEE Graduate Teaching Award in 1998, and the IEEE Millennium Medal as well as the IEEE CAS Golden Jubilee Medal in 2000.