A 110 dB CMRR/PSRR/gain CMOS Operational Amplifier

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***Abstract* — A CMOS operational amplifier with 110 dB CMRR/PSRR/gain is described. High CMRR is achieved using the cascoded input stage with high output impedance tail current source. A lateral PNP transistor and low-threshold voltage MOS transistor are used to create the voltage source stabilizing the drain-source voltage of input transistors. Common-mode input signal range includes negative rail voltage. The high stability self-regulated bias PTAT core is used to improve PSRR. The amplifier comprises two gain stages connected via cascoded current mirror with voltage gain boost. The output class AB stage is using local feedback control of the reference voltages, and has an improved quiescent current vs. supply voltage stability.**

***Key words*: operational amplifiers, CMRR, PSRR, gain boost, cascoding, lateral p-n-p transistors, low-threshold voltage MOS transistor.**

I. Introduction

The operational amplifiers (OpAmps), implemented in the generic CMOS technologies, have CMRR/PSRR that is usually in the range of 75-85 dB. Goal of this project was to improve these figures up to 110 dB, and, at the same time, to preserve the single-supply capability (i.e. common-mode input signal range including the negative rail voltage), the rail-to-rail IO operation, and high open-loop gain of 110 dB while keeping high speed to power ratio of the two-gain-stage OpAmp structure.

To achieve this goal, transistors of the input differential pair operate in the "greenhouse" conditions: their drain-source voltages are stabilized using p-n-p lateral cascoding transistors and voltage source, which includes lateral PNP transistor and low-V_{th} or "natural" (the jargon term for the NMOS transistors without V_{th} adjustment layer) n-MOS transistor. This approach also boosts the input stage output impedance, and insures that the voltage offset and noise of the next stage does not cause any input-related errors.

The major factor defining the CMRR is the tail current source output impedance [1]. Hence, the variation of the input pair tail current source in the input signal common range can significantly harm CMRR (although it is very hard to simulate this variation). Here we propose the tail current source with internal feedback loop improving the output impedance and voltage compliance range of the source.

Improvement of the OpAmp PSRR is accomplished using a self-subregulated PTAT biasing core.

High open-loop gain of the OpAmp is achieved using the nested gain boost in the folded cascoded current mirror.

Stability versus supply voltage of the quiescent current, I_q, in the Class AB output stage is achieved by the feedback control of the reference voltages.

The whole design was done using the structural design approach [3], where the main mean to achieve any important system parameter or characteristic is dedicated and efficient feedback loop controlling this parameter or characteristic.

Part II of the paper describes the input stage and measures that improve CMRR. Part III outlines the schematic of the self-subregulated PTAT biasing core. Part IV describes improvement in the folded cascode stage to increase the open-loop OpAmp gain. Part V shows feedback control of the reference voltages in the class AB output stage. Part VI describes the experimental results. Finally, Part VII draws some conclusions.

II. Input Stage Design

The PMOS input stage schematic is shown in Fig. 1. To improve CMRR, the input PMOS differential pair operates with a stable tail current as well as with the constant source-drain, V_{SD}, and source-body, V_{SB}, voltages. Constant V_{SD} of the input transistors M_0 and M_1 is defined by a voltage source V_0 consisting of the current source I_2, lateral PNP transistor Q_2 and a low-V_{th} n-MOS transistor M_2.

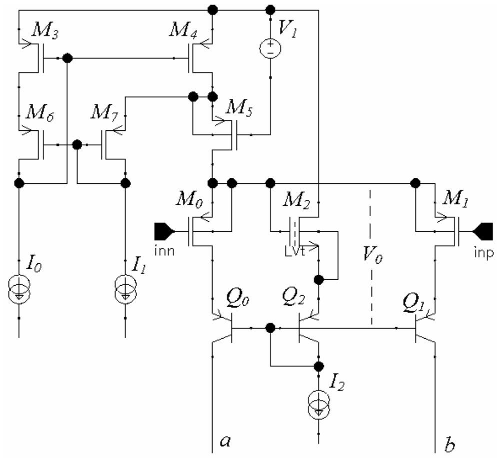

Fig.1. Input stage cascoding and tail current source

As the source-gate voltage, V_{SG}, of PMOS transistors is larger than the emitter-base voltage, V_{BE}, of bipolar transistors, some voltage headroom for the source I_2 exists even when common-mode input voltage is at the negative rail. I_2 keeps V_0 stable, and the stage is operational even in this condition. V_{GS} of M_2 defines V_{DS} of the input transistors; this V_{DS} should be larger than 100 mV to keep input devices out of triode operation but smaller than ($V_{GSM0,1} - V_{BE}$). V_{th} of the "natural" NMOS transistors in the process used is located conveniently in this "right" range of 150-200 mV.

Cascoding of the input transistors also increases the stage output impedance, thus, ensuring that the voltage offset or noise at the input of the next stage (folded cascode) does not cause the input-related error [4].

The tail current source for the input stage comprises the cascoded current mirror M_3, M_4, M_5 with the feedback loop using the current-input amplifier M_6, M_7. This control loop keeps the drain voltages of M_3 and M_4 equal even when the tail voltage is approaching positive rail and M_5 enters the triode operation. The loop operation ensures matching of M_3, M_4 currents even when the tail voltage is only 50 mV from the positive rail.

The OpAmp also has a NMOS input stage (not shown) that becomes operational when the common-mode input voltage is close to the positive rail. This stage is not designed for high accuracy and added only in order to preserve some OpAmp functionality in this range and to avoid the conditional instability or other undesirable effects in applications.

III. Biasing Core

OpAmp PSRR can not be reliably simulated with existing software and models. The discrepancy between PSRR simulation and experimental results often exceeds one order of magnitude. But, by the common sense, the variation of the biasing currents by the supply voltage is the major reason of low PSRR value, and the PSRR improvement may be accomplished using a high stability bias core source.

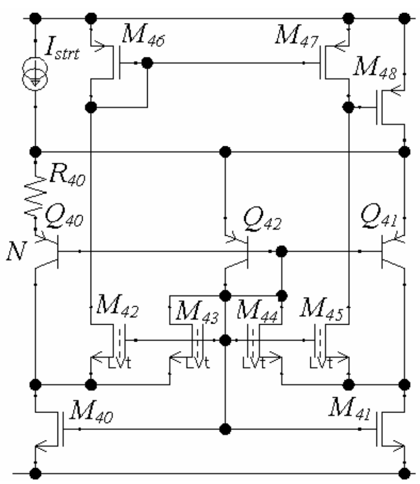

Fig. 2. Self-subregulated PTAT biasing core

Such self-subregulating PTAT current source is shown in Fig. 2. It comprises the lateral transistors Q_{40}, Q_{41}, Q_{42}, the current mirror M_{40}/M_{41}, and the feedback current-input amplifier implemented by the low-V_{th} transistors M_{42}, M_{43}, M_{44}, M_{45} (input stage), current mirror M_{46}/M_{47}, and output transistor M_{48}. As any PTAT bias core, this circuit has positive (M_{48}-Q_{40}-M_{42}-M_{47}) and negative (M_{48}-Q_{40}-M_{45}) feedback loops. Gain in the positive loop is larger on small currents, and negative loop prevails at larger currents. At the equilibrium point the collector currents of Q_{40} and Q_{41} are equal to I_C, that is

$$I_C = (V_t \ln N) / R_{40} \,. \quad (1)$$

Here V_t is the p-n junction thermal voltage (~26 mV at the room temperature), and N is the emitter area ratio for Q_{40}/Q_{41}. The voltage at the drain of M_{48} is equal to ($V_{BE}+V_{GS40,41}$). During the steady-state operation, all transistors, whose matching and operation point stability is important for accuracy, function in the stable or at least in matching conditions: $V_{CE40} \approx V_{CE41} = V_{BE}$, $V_{DS40} = V_{DX41} \approx V_{th40}$-$V_{th43}$ = *const* and $V_{DS42} \approx V_{DS45}$. Operation point variation vs. power supply voltage for Q_{40}, Q_{41}, M_{40} and M_{41} can be neglected. As a result, the variation of the I_C vs. supply is less than 0.2% in the range from 1.5 to 5.5V of the power supply voltage.

The negative feedback loop has only one gain stage (M_{48}) and does not require compensation capacitors. This bias core needs a start-up current source I_{strt}.

IV. Folded Cascode

The folded cascode stage (Fig. 3) comprises current mirrors M_{12}/M_{13} and M_{14}/M_{15} with cascoding transistors M_{10} and M_{11} and source degeneration resistors R_{12}-R_{15}. The amplifiers A_{11} and A_{12} boost the stage output resistances seen at the nodes *c* and *d* [5]. The stage employs the floating current source that is obtained using M_{16} with the feedback amplifier A_{10} and the reference branch I_{10}/M_{17}.

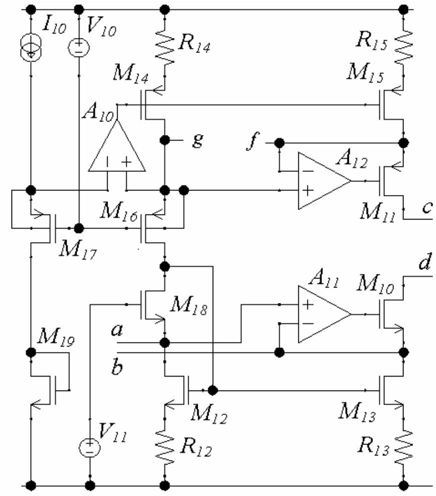

Fig. 3. Folded cascode stage with gain boosts and floating current source

The outputs of PMOS input stage (Fig. 1) are connected to the nodes *a* and *b*; the drains of the NMOS input stage (not shown in Fig. 1 and Fig. 3) are connected to the nodes *g* and *f*. Using the floating current source allows one to get easy switching from PMOS to NMOS inputs, and independent choice of the input stage tail current and the current in the folded cascode.

In order to decrease the impact of folded cascode on the OpAmp speed, transistors M_{10} and M_{11} should operate in the medium/weak inversion (to maximize transconductance) and be of the minimal channel length (to minimize area and parasitic capacitances). The nodes *c* and *d* are connected to the gates of output transistors (Fig. 4). At high temperatures, and without load V_{GS} of the output NMOS and the voltage at the node *d* can drop to 400mV. Indeed (Fig. 3), with at least 200 mV of V_{DS13} (operation of the mirror transistors in the triode region would significantly increase the OpAmp noise), and at least 100 mV across R_{13} (also necessary for the noise improvement), V_{DS10} can be as low as 100 mV and M_{10} may operate in the triode region. The equivalent resistance at the gates of output devices (nodes *c* and *d* of Fig. 4) limits the open-loop gain of the considered OpAmp. With all these considerations, to achieve a 120 dB OpAmp gain, while M_{10} is in the triode region of operation, the voltage gain of the boost amplifier A_{11} (Fig. 3) should be at least 100 dB.

The schematic of amplifier A_{11}, satisfying this requirement, is shown in Fig. 5. The amplifier consists of the differential pair M_{30}/M_{31} with the load current mirror M_{32}/M_{33}, and the cascoding transistor M_{34}. Transistor M_{35} boosts the resistance seen at the drain of M_{34} in the same way as A_{11} boosts the resistance seen at the drain of M_{10}.

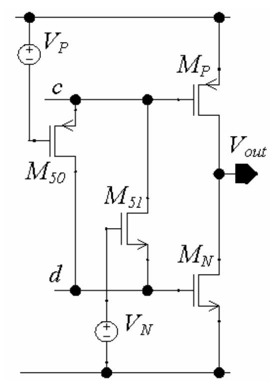

Fig. 4. Class AB output stage

The gain requirement to A_{12} is not as strict as V_{GS} of the PMOS output device is larger and M_{11} does not need to operate in the triode region.

V. Output Stage

The class AB output stage of this amplifier (Fig. 6) includes the feedback control of the reference voltages [3]. The preceding folded cascode stage of Fig. 3 is connected by joining of the nodes *c* and *d* to the same nodes of Fig. 6.

Comparative simulations of the OpAmp schematics quickly demonstrate that the achievable bandwidth of this two-gain-stage structure OpAmp is limited, in the first approximation, by the size (hence, the parasitic capacitances) of the output transistors M_N and M_P. To decrease the transistor area while providing the required load current, the channel length of M_N and M_P should be chosen minimal. In the circuit of Fig. 6, when transistors M_{50} and M_{51} have constant gate voltages V_P and V_N while M_N and M_P have 0.6 um channel length only, the quiescent current of the output stage may vary 3 - 4 times in the supply voltage range from 1.8 to 5.5V. The output stage quiescent current, I_q, represents more than a half of the total OpAmp current budget, and such variation is not acceptable.

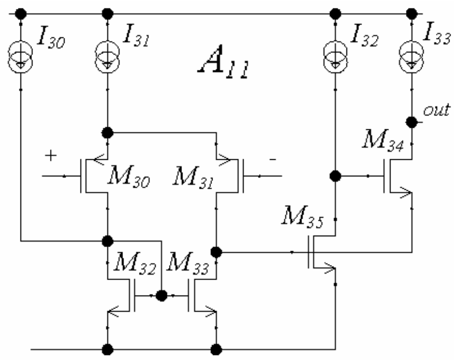

Fig. 5. Gain boosted gain boost amplifier

This variation can be diminished if these reference voltages V_P and V_N are controlled with dedicated feedback loops. The loop for V_P is shown in Fig. 6.

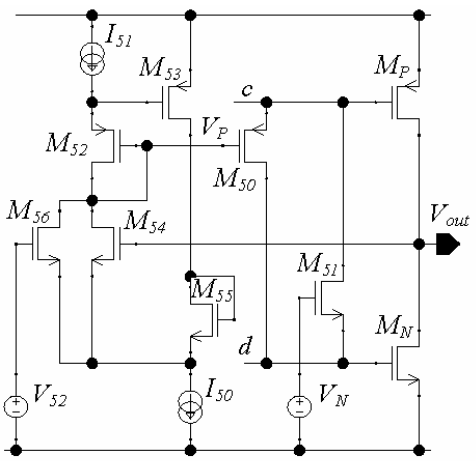

Fig. 6. Feedback control of the reference voltage in class AB output stage

This feedback loop consists of the transistor M_{52} matching M_{50}, M_{53} matching M_P, transistors M_{54}, M_{55} and the current sources I_{50} and I_{51}. During operation without load, the current through M_{53} is equal to I_{51}-I_{50} (a convenient choice is $I_{51}=2I_{50}$), the current through M_{52} is equal to I_{51}, and the source-drain voltage of M_{53} is nearly equal to the source-drain voltage of M_P. If the output voltage changes, the voltage V_{50} now slightly changes as well, as the voltage at the drain of M_{53} follows the voltage at the drain of M_P. The operating conditions for M_{53} and M_P are matching. The drain current of M_{53} is constant, and the M_P current, as well as I_q of output stage, is defined by the size ratios of M_{53} to M_P and M_{52} to M_{50}. The gate voltage (V_N) of M_{51} is controlled in the same way, and, as a result, the quiescent current I_q of the stage is stable vs. supply and output voltage variations.

The clamp circuit M_{56} and V_{50} keeps the feedback loop operational when the output voltage is close to negative rail.

VI. Experimental Results

The amplifier was manufactured in the Texas Instruments 50HPA07 process with 0.6μm minimum channel length. The amplifier occupies 730x710 μm^2 die area and fits SC-70 package. CAD die picture is shown in Fig. 7.

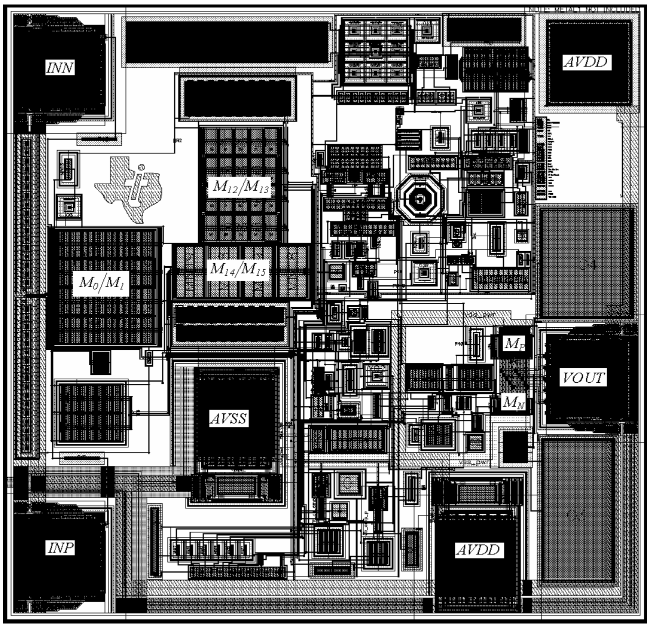

Fig. 7. OpAmp layout

As the offset and flicker noise are inversely proportional to the root square of size, the largest devices on the die are the input pair M_0/M_1 and the transistors of the folded cascode mirrors M_{12}/M_{13} and M_{14}/M_{15}.

The OpAmp is capable to drive up to 10 mA loads, but the output devices M_P/M_N are relatively small due to their short channel. The additional bondpad for positive supply allows the placement in all industry-standard packages.

The measured parameters of the OpAmp are summarized in Table 1.

Table 1. OpAmp Parameters

	Min	Typ	Max
Total supply voltage, V	1.8		5.5
Quiescent current, μA		3	5
Unity-gain bandwidth, kHz		120	
CMRR, 0 to (VDD-1V), μV/V		1	3
PSRR, μV/V		1	3
Open loop gain, RL=5k, dB	110		
Noise, 1 kHz, nV/sqrt Hz		100	
Noise, p-p, 0.1 to 10 Hz, μV		8	
Slew rate, V/ms		20	
Voltage offset, mV		0.2	1

VII. Discussion and Conclusions

The obtained result is confirming once more the validity of structural design approach for solving the problems in the electronic system design. By its CMRR/PSRR parameters this OpAmp is not only superior to the typical industrial OpAmps [2], but it is approaching the auto-zeroing or chopper amplifiers, with excluding the penalties of high power consumption, abnormal settling or switching noise.

This OpAmp comprises more than 20 local feedback loops, but the only frequency compensation components are capacitors of the overall OpAmp Miller compensation (shown above and below *VOUT* pad in Fig. 7). This feature is achieved using only single-gain stage amplifiers in these local loops.

References

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