

Mismatch Shaping for a Current-Mode Multibit Delta-Sigma DAC

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Abstract—Mismatch shaping allows the use of multibit quantization in delta-sigma analog-to-digital converters and digital-to-analog converters (DAC's) since it noise-shapes the error caused by static element mismatch in a multibit DAC. In this paper, mismatch-shaping techniques for low-pass delta-sigma ($\Delta\Sigma$) modulators are reviewed, and a mismatch-shaping technique for bandpass $\Delta\Sigma$ modulators is described. The dynamic error caused by frequent element switching is identified as a major source of error in a current-mode DAC with a continuous-time output. Modifying the mismatch-shaping algorithm to account for this effect yields a continuous-time $\Delta\Sigma$ DAC that is insensitive to both element mismatch and element switching dynamics. Experimental results confirm the effectiveness of the proposed techniques.

Index Terms—Current-mode circuits, delta-sigma modulation, digital-analog conversion, mismatch shaping.

I. INTRODUCTION

ONE-BIT $\Delta\Sigma$ modulators have been widely used in high-linearity, moderate-bandwidth data converters. A key feature of a 1-bit $\Delta\Sigma$ modulator is its ability to achieve perfect linearity by virtue of its 1-bit digital-to-analog converter (DAC). In contrast, a multibit DAC cannot be made perfectly linear without the use of perfectly matched components. Since nonidealities in the DAC are equivalent to errors added directly to the input signal, the linearity of a $\Delta\Sigma$ analog-to-digital converter (ADC) is no better than that of its multibit internal DAC.

However, multibit $\Delta\Sigma$ converters possess two important advantages over single-bit converters. The first advantage is that much higher performance is possible through the use of a more aggressive noise transfer function (NTF). For example, a fifth-order binary modulator operated at an oversampling ratio (OSR) of 16 can achieve a signal-to-noise ratio (SNR) of at most 60 dB [1]. However, by increasing the number of quantization levels to eight and designing for a more aggressive NTF, simulations indicate that 108-dB SNR can be achieved with the same modulator order and the same OSR. The second advantage is that the output of the modulator more closely resembles the desired output and contains much less out-of-band noise. This reduction in the out-of-band noise eases the burden on the postfiltering stage, reduces the sensitivity of the output to edge jitter, and relaxes the slew-rate requirements on the analog output stage. These advantages have driven a number of researchers to develop such schemes

as dynamic element matching [2], [3], digital calibration [4], [5], individual level averaging [6], [7] and mismatch shaping [8]–[17] to combat the problems caused by DAC nonlinearity.

Although discrete-time implementations of $\Delta\Sigma$ modulators are the most common, continuous-time modulators are more attractive in high-speed applications. Continuous-time modulators can benefit from the use of multibit quantization in the same way as discrete-time modulators. Unfortunately, both static and dynamic errors are severe sources of performance degradation in a multibit continuous-time modulator. This paper shows that it is possible to noise-shape static errors and simultaneously reduce certain dynamic errors, simply by modifying the element-selection algorithm.

The next section briefly reviews the principles and algorithms associated with low-pass mismatch shaping. Section III describes an efficient algorithm for bandpass mismatch shaping, while Section IV covers the modified mismatch-shaping algorithm for continuous-time multibit $\Delta\Sigma$ modulators. Section V describes a current-mode unit-element DAC, which was used to verify the preceding algorithms. Experimental results are presented in Section VI, and Section VII summarizes this work.

II. MISMATCH-SHAPING REVIEW

A. Mismatch-Shaping Principle

Fig. 1 shows the block diagram of a general mismatch-shaping system described in [14]. The output of a $\Delta\Sigma$ modulator produces an $M + 1$ level signal $v(n)$, which is fed into the mismatch-shaping logic block. The $sv(n)$ output of the block contains M bits, each of which enables a particular unit element in the subsequent unit-element DAC. The number of elements enabled at each instant is equal to $v(n)$. The mismatch-shaping logic of Fig. 1 selects elements in such a way that the mismatch error existing between those elements is noise shaped, much as a $\Delta\Sigma$ modulator shapes quantization noise.

Analyzing the system shows that the output of the DAC is

$$DV(z) = kV(z) + H_2(z)DE(z) \quad (1)$$

where k is the average element value, $V(z)$ is the output of the modulator, $DE(z)$ is an error signal introduced by element mismatch, and $H_2(z)$ is the mismatch transfer function (MTF). The key point is that the error due to element mismatch is shaped by the MTF, even though the actual element values are unknown. More detailed descriptions of this and other mismatch-shaping techniques are given in [18].

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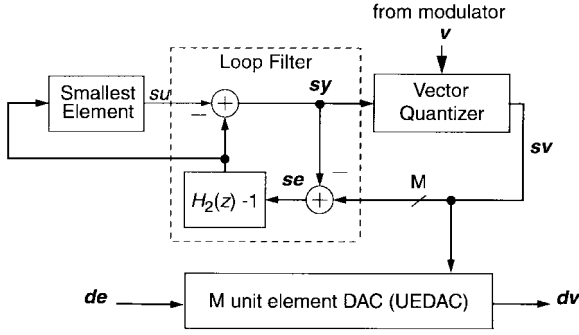


Fig. 1. A general diagram of mismatch shaping.

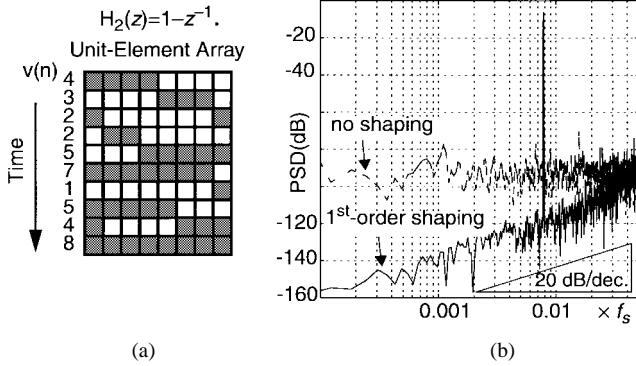


Fig. 2. Element rotation algorithm for an eight-element DAC: (a) element selection pattern and (b) simulated result with a third-order modulator.

B. Example: First-Order Low-Pass Mismatch Shaping

First-order low-pass mismatch shaping uses the MTF

$$H_2(z) = 1 - z^{-1} \quad (2)$$

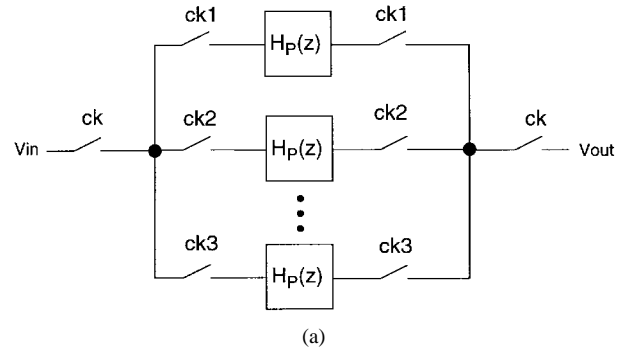
and can be implemented by the element rotation scheme [8], [10] depicted in Fig. 2(a). (This scheme is also known as data-weighted averaging [11], [12].) In this algorithm, the unit elements are selected in a rotational manner. This operation is equivalent to differentiating a signal related to the integral nonlinearity of the DAC and results in first-order shaping. As shown in Fig. 2(b), the mismatch-induced noise present in the output of a $\Delta\Sigma$ DAC is first-order shaped (i.e., it has a 20-dB/decade slope) in the low-frequency band.

III. MISMATCH SHAPING FOR BANDPASS $\Delta\Sigma$ MODULATORS

A bandpass delta-sigma modulator benefits from multibit quantization in the same way as its low-pass counterpart: wider input dynamic range and better stability, much higher performance, and closer resemblance of the desired output in the time domain. However, as is the case with a low-pass modulator, the linearity and SNR of a multibit bandpass modulator is limited by the DAC. In this section, several existing schemes for bandpass mismatch shaping are reviewed, and an efficient mismatch-shaping scheme that has improved performance is presented.

A. Existing Bandpass Mismatch Shaping

In [17], Henderson and Nys showed one way to implement a second-order mismatch-shaping transfer function for a band-

Fig. 3. (a) N -path filter principle. (b) Frequency response of a four-path differentiator.

pass delta-sigma modulator that has center frequency at $f_s/4$. The sought-after mismatch-shaping function is

$$H_2(z) = 1 + z^{-2}. \quad (3)$$

Although the effectiveness of the approach was demonstrated in simulation, the method suffers from two drawbacks. First, it requires several steps in each cycle to generate the element selection bits. Second, the implementation requires a considerable amount of digital hardware.

Lindfors *et al.* [19] and Hernandez *et al.* [20] described an efficient mismatch-shaping scheme for multibit bandpass delta-sigma modulators. The method is based upon application of the N -path filter principle to the element rotation scheme, as shown in Fig. 3(a). In this figure, each path implements a first-order high-pass transfer function

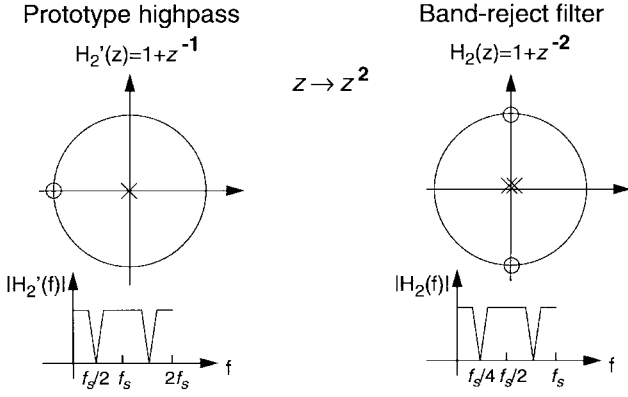
$$H_P(z) = 1 - z^{-1}. \quad (4)$$

Each clock frequency equals f_s/N , where the system clock frequency is f_s . By using four path filters in parallel, the overall transfer function becomes

$$H(z) = 1 - z^{-4}. \quad (5)$$

Thus, four zeros (notches) are obtained by the four-path filtering transformation from (4) and (5). The frequency response of $H(z)$ in (5) is shown in Fig. 3(b). The zeros at $f_s/4$ and $3f_s/4$ can suppress the mismatch noise in the band of interest of a bandpass delta-sigma modulator with center frequency $f_s/4$.

This scheme can perform the element selection in a single cycle. Compared with the algorithm in [17], this four-path method can be implemented more efficiently and higher speed can be obtained. However, this algorithm has one drawback: the MTF has four zeros spread around the unit circle, and only the two zeros at $f_s/4$ and $3f_s/4$ are useful in reducing the mismatch noise in the band of interest. The existence of two

Fig. 4. Two-path transformation of $H_2(z)$.

unwanted zeros (at dc and $f_s/2$) degrades the effectiveness of the mismatch shaping by 6 dB.

B. Improved Bandpass Mismatch Shaping

To effectively shape the noise in the band of interest caused by mismatch error, the MTF should be $H_2(z) = 1 + z^{-2}$. While an efficient implementation of H_2 is not obvious from the structure depicted in Fig. 1, a simple and effective scheme can be achieved if we first consider implementing

$$H'_2(z) = 1 + z^{-1}. \quad (6)$$

A two-path transformation $z \rightarrow z^2$ on H'_2 will implement the desired MTF [21]. Fig. 4 illustrates the principle of this two-path transformation: the zeros of $H'_2(z)$ at $z = -1$ are mapped to $z = \pm j$, providing the desired notch at $f_s/4$. One way to implement H'_2 is shown in Fig. 5(a). Rather than rotating forward into the least recently used elements as in the element rotation scheme, rotate back and forth through the most recently used elements. The reason for reusing the most recently used elements is that the impulse response of the H'_2 is $\{1, 1\}$, indicating that the errors made in the last step need to be repeated.

Fig. 5(b) shows simulation results for a third-order 17-level bandpass modulator with a tone input. In the absence of element mismatch, this modulator achieves 96-dB SNR at an OSR of 32. With 1% mismatch, the SNR drops to 62 dB if mismatch shaping is not used, but rises to 90 dB if the element selection strategy described above is employed. The two-tone test results presented in Fig. 6 confirm that the spurious-free dynamic range is also improved when mismatch shaping is applied.

IV. MODIFIED MISMATCH SHAPING

A. Motivation

Mismatch shaping can yield a highly linear DAC if the DAC errors are dominated by static mismatch. Unfortunately, no benefit is accrued when the DAC performance is dominated by dynamic errors. In fact, since mismatch shaping generally increases the element switching activity, it can actually increase the noise and spurs caused by nonideal element dynamics.

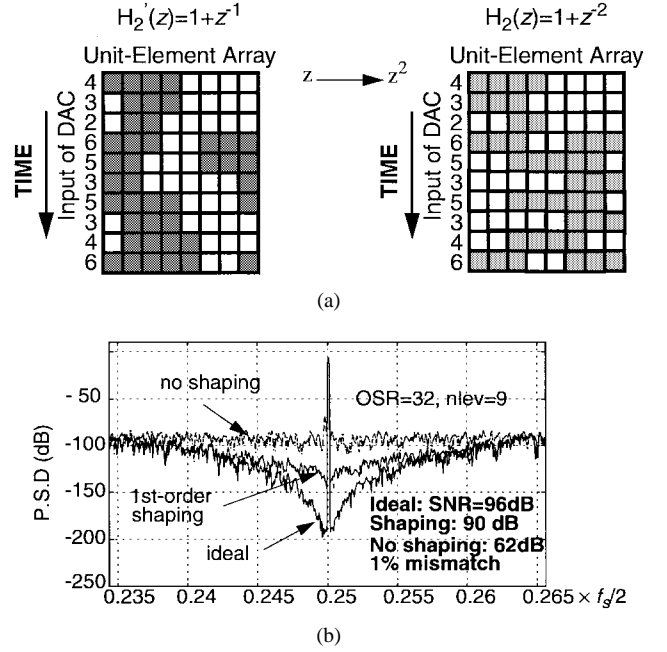


Fig. 5. Bandpass mismatch shaping for an element example: (a) selection algorithm and (b) simulation results.

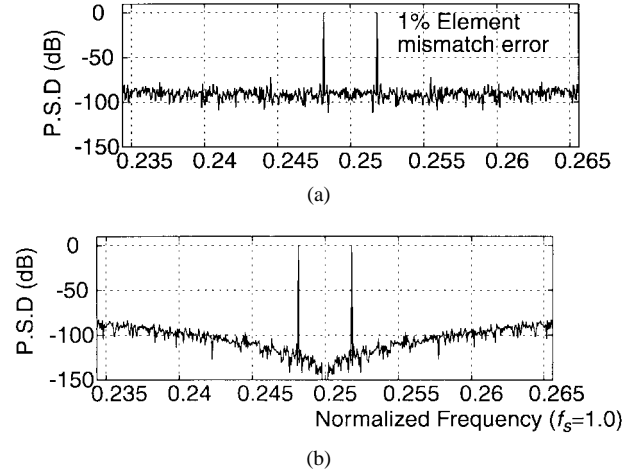


Fig. 6. Bandpass modulator with two-tone simulation: (a) no shaping and (b) mismatch shaping.

In a DAC with a continuous-time output, the error induced by turning an element on or off is a serious source of noise and distortion. Differences between the on and off delays on the order of a few tens of picoseconds are significant at output frequencies in the tens of megahertz. Even if the on and off delays are precisely equal, matching of the rise and fall times is similarly critical. Using the return-to-zero method is one way to address nonideal settling dynamics, but doing so eliminates the aforementioned advantages associated with a smooth time-domain waveform: namely, reduced sensitivity to edge jitter and slew rate distortion.

B. Dynamic Error Model

A simple model for analyzing the effect of unequal on/off delay is shown in Fig. 7. The delay time error is modeled as a gain factor $\Delta\tau$, which can only be seen at the output

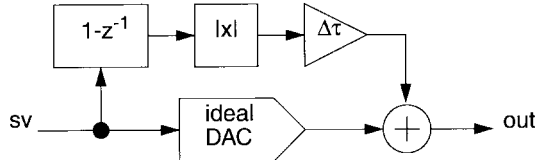


Fig. 7. Discrete-time model for unequal on/off delay.

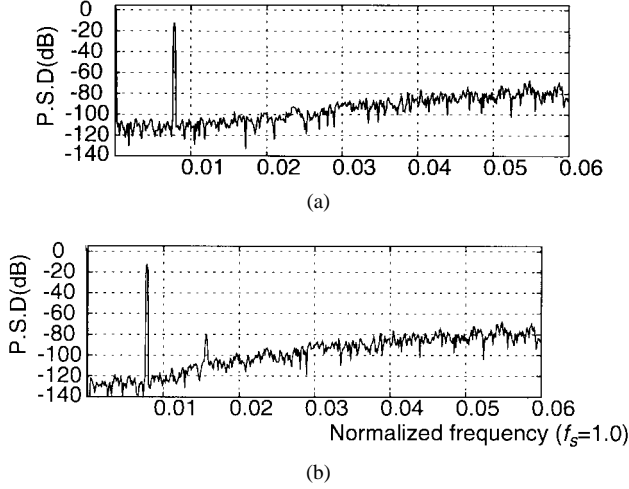


Fig. 8. Simulation results for the discrete-time model: (a) no shaping and (b) first-order shaping. The dynamic error is assumed to be 0.1%.

when the number of elements turned on or off is nonzero. The number of elements that switch is denoted as $|x|$ in this figure. According to this model, the instantaneous error is proportional to the total number of switching events that occur in each sampling interval but is independent of whether elements are being turned off or turned on. A similar model based on analysis of the time-domain waveforms is presented in [23], but this more complex model collapses to that shown when second-order effects are ignored. Both models assume that the switching dynamics of all elements are identical.

Fig. 8 shows the results of simulations using the model in Fig. 7. A third-order low-pass modulator with nine-level quantization employing no-shaping and first-order mismatch shaping is used to generate the sv vector. It is assumed that no mismatch exists in the unit element DAC, but that the on and off delays differ by 0.1% of a clock period. The generation of a second-order harmonic (especially visible in the first-order shaping case) is due to the absolute function $|x|$, which generates even-order harmonics. Since first-order shaping tends to switch elements more frequently, the shaping result is more sensitive to dynamic errors than the no-shaping case.

C. Algorithm

The idea underlying modified mismatch shaping (MMS) is similar to that of $\Delta\Sigma$ modulation: make the spectrum of the switching error harmless. A particularly simple form of this idea is to set the number of switching events per period to a constant. This choice turns the errors caused by nonideal element dynamics into a dc offset.

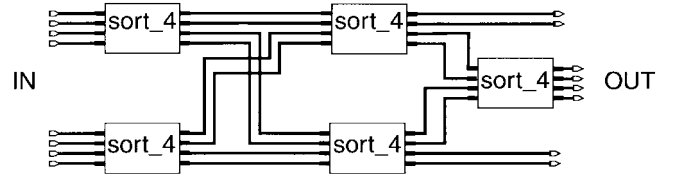


Fig. 9. Partial-sorting block used in the vector quantizer for an eight-element MMS DAC.

To see how such a selection strategy can be implemented, let $v(n)$ (a positive number) be the output of a $\Delta\Sigma$ modulator. Define rem , on , and off as the number of elements that remain on, are turned on, or are turned off at time step n , respectively. Last, let L be the number of elements required to switch at each time step. Therefore

$$on - off = v(n) - v(n-1) \quad (7)$$

$$on + off = L \quad (8)$$

$$rem + on = v(n). \quad (9)$$

By solving these equations, we have

$$on = (L + v(n) - v(n-1))/2 \quad (10)$$

$$off = (L - v(n) + v(n-1))/2 \quad (11)$$

$$rem = (v(n) + v(n-1) - L)/2. \quad (12)$$

For fixed L , the physical constraints $on \geq 0$, $off \geq 0$, and $rem \geq 0$ result in restrictions on the input sequence $v(n)$. However, by allowing L to vary about a target value, these restrictions can be lifted. Furthermore, if the L sequence is endowed with a noise-shaped spectrum, the errors caused by nonideal dynamics are also noise shaped.

The implementation of MMS follows the diagram of Fig. 1, except that the vector quantizer must now operate under more constraints. In addition to the usual requirement that the number of elements enabled at time n must be $v(n)$, the vector quantizer must also attempt to satisfy (10)–(12). The procedure adopted is as follows.

- 1) Calculate on , off , and rem using (10)–(12).
- 2) If one of on , off , or rem is negative, set it to zero and choose L such that (7)–(9) are satisfied. This requires recomputation of two of on , off , and rem .
- 3) From the elements that are off, select the on elements having the largest $sy(n)$ components.
- 4) From the elements that are on, deselect the off elements having the smallest $sy(n)$ components.

To implement the above procedure, it would appear that the vector quantizer requires a sorted and indexed $sy(n)$ vector. Since a circuit that performs a one-step sort is complex, this requirement is not easily met, especially at high speeds or with large numbers of elements. Fortunately, the MMS algorithm can operate with a partially sorted $sy(n)$ vector, such as that produced by the circuit whose block diagram is shown in Fig. 9. The tree-sorting approach of [24] and [25] is another candidate for performing a hardware-efficient partial sort.

Fig. 10 shows an example of the element usage pattern under MMS. Here, the initial value of L is four. It can be

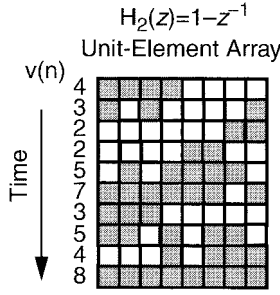


Fig. 10. Element selection pattern with MMS.

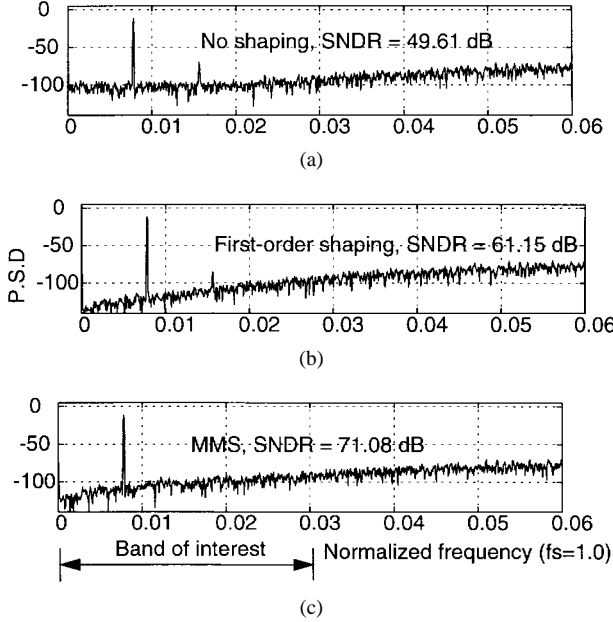


Fig. 11. Simulation results for (a) no mismatch shaping, (b) first-order shaping, and (c) MMS.

seen that the number of elements that switch at each time step is fairly constant (either three or four). Since the number of elements that switch is not fixed, the dynamic error is not truly constant. To make the number of elements that switch constant, the output of the driving modulator must be restricted, as mentioned earlier. Since such constraints reduce the resolution of the multibit quantizer, the number of elements that switch has been allowed to vary.

MATLAB simulations have been performed, and one of the simulation results is shown in Fig. 11. Here, a third-order $\Delta\Sigma$ modulator with nine-level quantization is used to generate $v(n)$. The DAC is assumed to have 1% mismatch error and 0.1% dynamic error. In this example, MMS outperforms standard mismatch shaping by 10 dB.

V. CURRENT-MODE DAC DESIGN

A current-steering DAC employing 16 nominally equal current sources and an off-chip resistor load is used as the testbed for the proposed mismatch-shaping algorithms. As shown in Fig. 12, each current source includes a single-ended switch driver (m1, m2), a cascode current source (m3, m4), and a local biasing network (m5 ~ m11). The single-ended switch driver allows adjustment of the threshold level

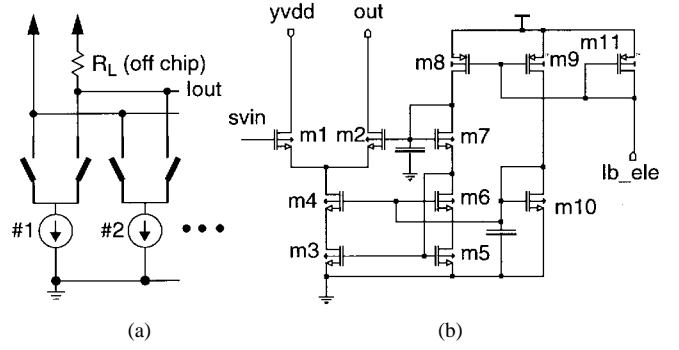


Fig. 12. Current-mode DAC: (a) system diagram and (b) unit-element schematic.

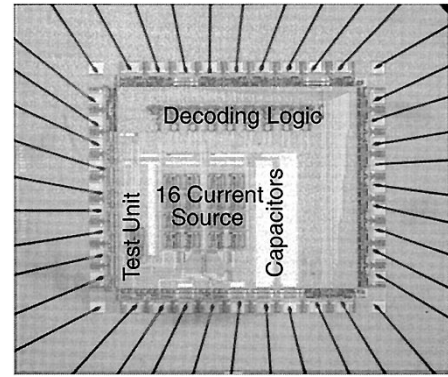


Fig. 13. Chip microphotograph.

of the input switch, thereby providing some control over the on/off delay difference. The cascode transistor yields a high output impedance, eliminating the noise and distortion caused by finite output impedance. The local biasing network provides isolation between elements, as element crosstalk can be another source of error. The DAC is fabricated in the Orbit 1.2- μm CMOS N-well double-poly double-metal process. Fig. 13 shows the microphotograph of the designed DAC.

VI. EXPERIMENTAL RESULTS

A third-order low-pass $\Delta\Sigma$ modulator with nine-level quantization is implemented on an XC4010E field-programmable gate array (FPGA). The modulator structure is as shown in Fig. 14(a). The test setup is shown in Fig. 14(b). Various forms of mismatch-shaping logic (first-order low-pass mismatch shaping, bandpass mismatch shaping, and MMS) are implemented using the FPGA.

A. Low-Pass Mismatch-Shaping Test

First, the performance of the DAC is evaluated with first-order low-pass mismatch shaping. Example test results are shown in Fig. 15. When no shaping is used, the observed harmonic distortion is $HD_2 = -60$ dB and $HD_3 = -65$ dB. After mismatch shaping is applied, HD_3 decreases by 20 dB, but HD_2 decreases by somewhat less.

If HD_2 is measured as a function of the sampling frequency, the result is as shown in Fig. 16, where the measured no-

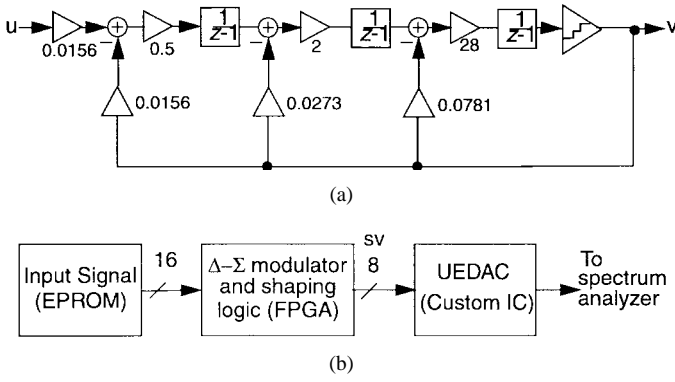


Fig. 14. (a) Block diagram of the third-order modulator. (b) Test setup.

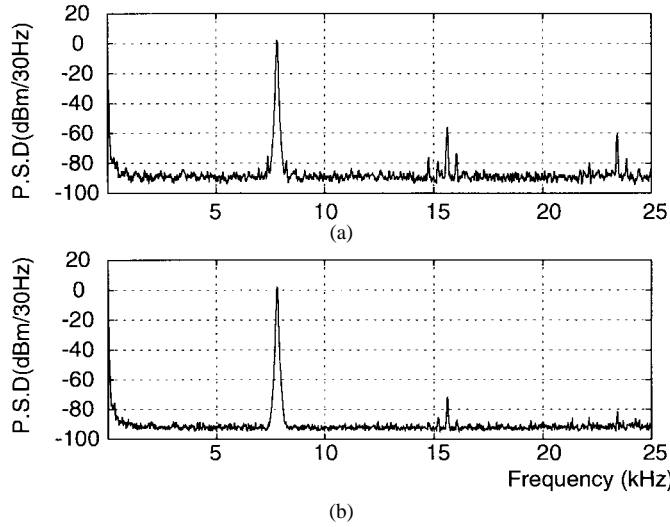


Fig. 15. Measured spectrum of UEDAC2 at $f_s = 500$ kHz: (a) no-shaping and (b) first-order shaping.

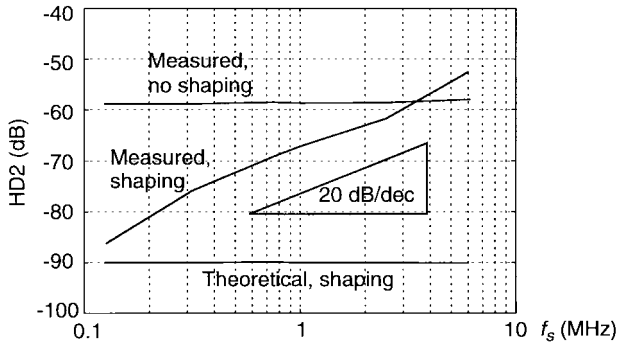


Fig. 16. Measured HD_2 of DAC as a function of the sampling frequency f_s .

shaping, measured first-order shaping, and theoretical first-order shaping curves are all plotted. The theoretical result comes from simulations of the DAC with element values taken from dc measurements. With first-order mismatch shaping applied, HD_2 is above the level predicted by simulations and is proportional to the clock frequency. For frequencies above 4 MHz, the shaped HD_2 actually exceeds the no-shaping level. This graph shows that dynamic effects dominate the shaped static mismatch error over the entire range of test frequencies.

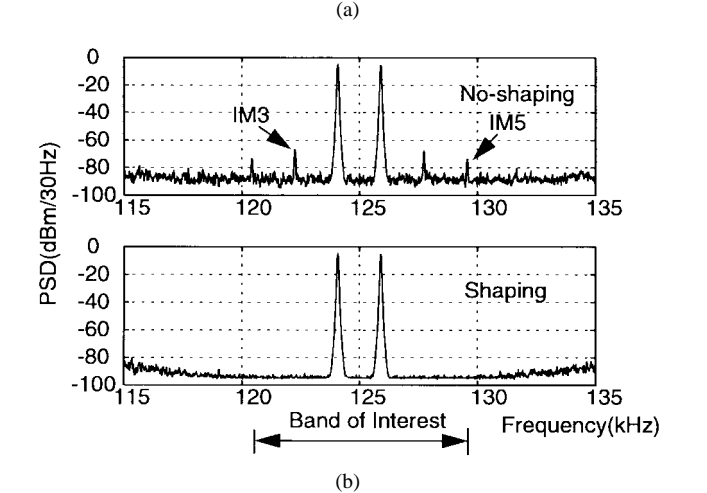
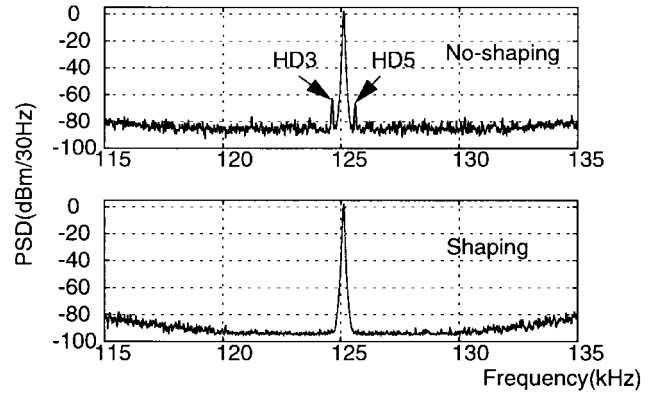


Fig. 17. Measured spectrum of bandpass Δ - Σ DAC at $f_s = 500$ kHz: (a) single tone and (b) two tone.

B. Bandpass Mismatch-Shaping Test

To test the effectiveness of the bandpass mismatch-shaping algorithm, a sixth-order bandpass modulator with nine-level quantization is implemented by applying a $z \rightarrow -z^2$ transformation to the prototype third-order low-pass modulator of Fig. 14(a). This bandpass modulator has its center frequency located at $f_s/4$ and preserves all the characteristic of the low-pass modulator (such as SNR, stability, etc.).

In Fig. 17(a), a single-tone test is performed. Because of folding, the third-order and fifth-order harmonics occur at offsets $-3\Delta f$ and $+5\Delta f$, respectively, where Δf is the offset of the fundamental from the center frequency $f_s/4$. With mismatch shaping, HD_3 and HD_5 are reduced from -64 dB and -69 dB, respectively, to less than -95 dB. The noise floor also decreases by about 14 dB. The proposed bandpass mismatch shaping appears to be effective. This is underscored by the results shown in Fig. 17(b) where the two-tone intermodulation products are found to be reduced by more than 20 dB.

C. Modified Mismatch-Shaping Test

As shown in Fig. 16, the linearity of the DAC employing first-order mismatch shaping is limited by the dynamic error, which was verified by adjusting the driver's threshold and observing the spurs' movement up and down.

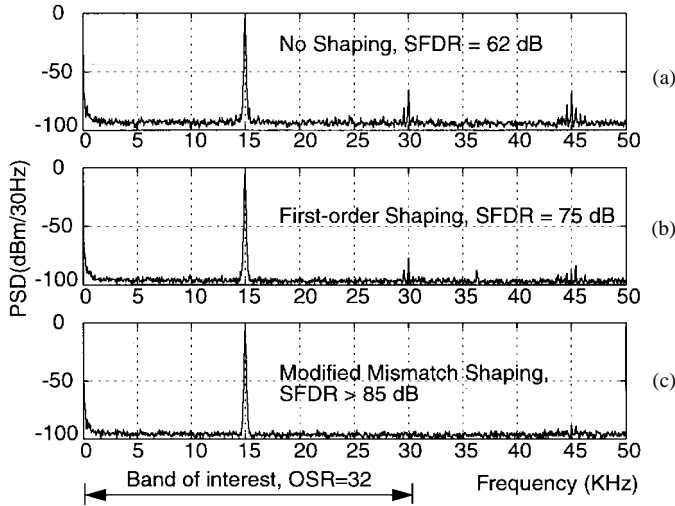


Fig. 18. Measurement from HP3585B spectrum analyzer when $f_s = 2$ MHz: (a) no mismatch shaping, (b) first-order shaping, and (c) MMS.

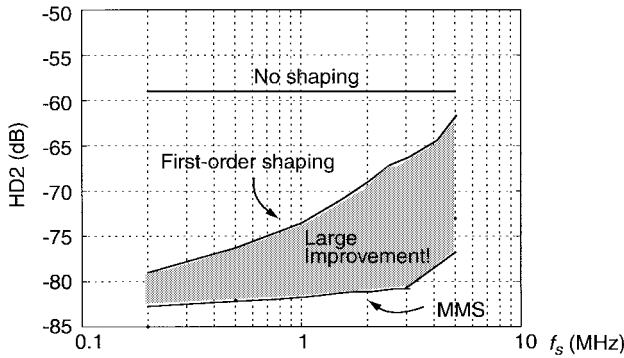


Fig. 19. Measured HD_2 versus sampling frequency with MMS.

The experimental result for $f_s = 2$ MHz is shown in Fig. 18. First-order mismatch shaping attenuates the noise floor and reduces harmonic distortion when compared with the no-shaping case, but HD_2 is still about -73 dB. After MMS is applied, the noise floor goes down and the harmonic distortion is virtually eliminated. Over 85 dB of spurious-free dynamic range is demonstrated.

Fig. 19 shows the measured HD_2 versus sampling frequency when MMS is applied. For comparison purposes, HD_2 with first-order shaping is plotted on the same graph. This graph shows that MMS yields a significant improvement, especially at high sampling frequencies.

The SNR of the DAC is measured with the help of a second-order notch filter to notch out the signal. Fig. 20 shows the measured spectra at $f_s = 500$ kHz. When no shaping is applied, mismatch error introduces a large amount of noise in the band of interest, and the notch filter's notch can be clearly identified in Fig. 20(a). When first-order mismatch shaping is applied, the in-band noise is limited by the notch filter, but 85-dB SNR can be measured. When MMS is applied, we can see there is a slight increase in the noise floor at the upper portion of the band of interest. This is due to the compromise inherent in the MMS algorithm: minimizing the dynamic effects causes a slight degradation in the effectiveness

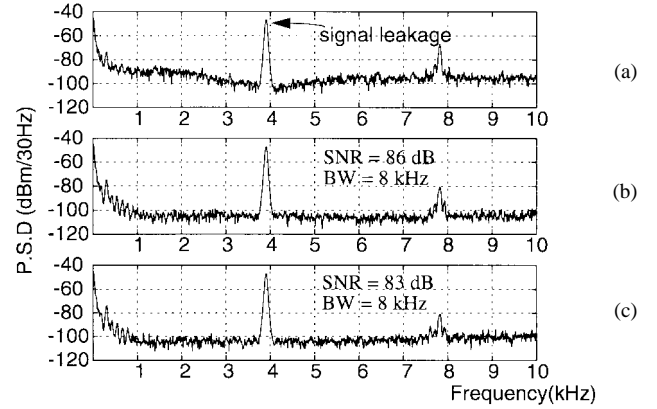


Fig. 20. Measured DAC spectrum after the notch filter: (a) no-shaping, (b) first-order shaping, and (c) MMS.

of the mismatch shaping. This results in an SNR of about 82 dB for MMS.

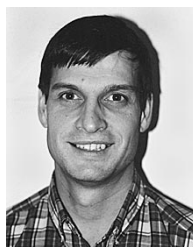
VII. CONCLUSIONS

A current-mode DAC is used to verify existing low-pass mismatch-shaping algorithms as well as the proposed band-pass and modified mismatch-shaping algorithms. Ordinary mismatch shaping is useful if the dominant DAC errors are due to element mismatch, but modified mismatch shaping is preferable when element switching dynamics dominate the mismatch-induced error.

REFERENCES

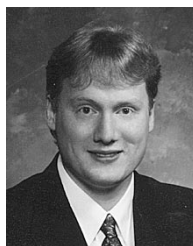
- [1] R. Schreier, "An empirical study of high-order single-bit delta-sigma modulators," *IEEE Trans. Circuits Syst. II*, vol. 40, pp. 461–466, Aug. 1993.
- [2] L. R. Carley and J. Kenney, "A 16-bit 4th order noise-shaping D/A converter," in *Proc. 1988 IEEE Custom Integrated Circuits Conf.*, Rochester, NY, May 1988, pp. 21.7.1–21.7.4.
- [3] L. R. Carley, "A noise-shaping coder topology for 15+ bit converters," *IEEE J. Solid-State Circuits*, vol. 24, pp. 267–273, Apr. 1989.
- [4] L. E. Larsen, T. Cataltepe, and G. C. Temes, "Multi-bit oversampled $\Sigma\Delta$ A/D converter with digital error correction," *Electron. Lett.*, vol. 24, pp. 1051–1052, Aug. 1988.
- [5] M. Sarhang-Nejad and G. C. Temes, "A high-resolution multi-bit $\Sigma\Delta$ ADC with digital correction and relaxed amplifier requirements," *IEEE J. Solid-State Circuits*, vol. 28, pp. 648–660, June 1993.
- [6] B. H. Leung and S. Sutarja, "Multi-bit $\Sigma-\Delta$ A/D converter incorporating a novel class of dynamic element matching," *IEEE Trans. Circuits Syst. II*, vol. 39, pp. 35–51, Jan. 1992.
- [7] F. Chen and B. H. Leung, "A high resolution multibit sigma-delta modulator with individual level averaging," *IEEE J. Solid-State Circuits*, vol. 30, pp. 453–460, Apr. 1995.
- [8] M. J. Story, "Digital to analogue converter adapted to select input sources based on a preselected algorithm once per cycle of a sampling signal," U.S. Patent 5 138 317, Aug. 11, 1992.
- [9] W. Redman-White and D. J. L. Bourner, "Improved dynamic linearity in multi-level $\Sigma\Delta$ converters by spectral dispersion of D/A distortion products," in *IEE Conf. Pub. Eur. Conf. Circuit Theory and Design*, Sept. 5–8, 1989, pp. 205–208.
- [10] H. S. Jackson, "Circuit and method for cancelling nonlinearity error associated with component value mismatches in a data converter," U.S. Patent 5 221 926, June 22, 1993.
- [11] R. T. Baird and T. S. Fiez, "Improved $\Delta\Sigma$ DAC linearity using data weighted averaging," in *Proc. 1995 IEEE Int. Symp. Circuits and Systems*, vol. 1, May 1995, pp. 13–16.
- [12] —, "Linearity enhancement of multibit $\Delta\Sigma$ A/D and D/A converters using data weighted averaging," *IEEE Trans. Circuits Syst. II*, vol. 42, pp. 753–762, Dec. 1995.
- [13] R. W. Adams and T. W. Kwan, "Data-directed scrambler for multi-bit noise-shaping D/A converters," U.S. Patent 5 404 142, Apr. 4, 1995.

- [14] R. Schreier and B. Zhang, "Noise-shaped multibit D/A convertor employing unit elements," *Electron. Lett.*, vol. 31, no. 20, pp. 1712–1713, Sept. 28, 1995.
- [15] I. Galton, "Noise-shaping D/A converters for $\Delta\Sigma$ modulation," in *Proc. 1996 IEEE Int. Symp. Circuits and Systems*, vol. 1, May 1996, pp. 441–444.
- [16] ———, "Spectral shaping of circuit errors in digital-to-analog converters," *IEEE Trans. Circuits Syst. II*, vol. 44, Oct. 1997, pp. 808–817.
- [17] R. K. Henderson and O. J. A. P. Nys, "Dynamic element matching techniques with arbitrary noise shaping functions," in *Proc. 1996 IEEE Int. Symp. Circuits and Systems*, vol. 1, May 1996, pp. 293–296.
- [18] R. Schreier, "Mismatch-shaping digital-to-analog conversion," in *103rd Convention Audio Engineering Society*, preprint no. 4529, Sept. 26–29, 1997.
- [19] S. Lindfors, P. Ööpik, K. Halonen, " N -path dynamic element matching for multibit Σ – Δ bandpass modulators," *Int. J. Circuit Theory Applications*, pp. 335–346, Sept.–Oct. 1997.
- [20] L. Hernandez and A. Quesada, "Programmable sine wave generator employing a mismatch-shaping DAC," in *Proc. 5th IEEE Int. Conf. Electronics, Circuits and Systems*, Sept. 1998, vol. 1, pp. 135–138.
- [21] T. Shui, R. Schreier, and F. Hudson, "Mismatch-shaping DAC for lowpass and bandpass multi-bit Δ – Σ modulators," in *Proc. 1998 IEEE Int. Symp. Circuits and Systems*, vol. 1, June 1998, pp. 352–355.
- [22] T. Shui, R. Schreier, and F. Hudson, "Modified-mismatch-shaping for continuous-time multi-bit Δ – Σ modulators," in *Proc. IEEE 1998 Custom Integrated Circuits Conf.*, June 1998, pp. 225–228.
- [23] T. Shui, "Lowpass and bandpass current-mode Σ – Δ DAC's employing mismatch-shaping," Ph.D. dissertation, Oregon State University, Corvallis, June 1998.
- [24] A. Yasuda and H. Tanimoto, "Noise shaping dynamic element matching method using tree structure," *Electron. Lett.*, vol. 33, pp. 130–131, Jan. 1997.
- [25] A. Yasuda, H. Tanimoto, and T. Iida, "A 100 kHz 9.6 mW multi-bit $\Delta\Sigma$ DAC and ADC using noise shaping dynamic elements matching with tree structure," in *ISSCC Dig. Tech. Papers*, Feb. 1998, pp. 64–65.



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