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Noise-shaped multbit D/A convertor employing unit elements

R. Schreier and B. Zhang

Indexing terms: Digital-analogue conversion, Sigma-delta modulation

By appropriately selecting the elements used to form each output sample of a multibit digital-to-analogue convertor, the spectrum of the error caused by element mismatch can be noise-shaped. Simulations indicate that first-order, second-order and bandpass noise-shaping are all possible. The technique enables the use of multibit feedback in delta-sigma A/D and D/A convertors.

Introduction: Delta-sigma modulation has emerged as an important method for converting signals from analogue to digital form and vice versa [1]. To realise a highly linear convertor, single-bit quantisation is often used. In a D/A convertor, single-bit quantisation requires that analogue circuitry filter a full-scale high frequency signal without introducing any distortion. Single-bit quantisation also puts severe constraints on the loop filter in high order A/D and D/A convertors, limiting their dynamic range.

Multibit quantisation is avoided because nonlinearity in the multibit D/A convertor translates directly into nonlinearity for the overall convertor. However, recently reported simulation results indicate that element mismatch errors in a multibit D/A convertor constructed from unit elements can be noise-shaped [2]. A related work [3] illuminated the operating principle and showed that first-order noise-shaping was the result. We generalise the approach and report simulation results for second-order and bandpass noise-shaping.

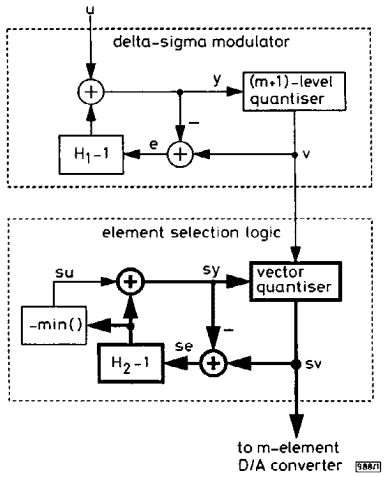

Fig. 1 *System diagram*

System diagram: Fig. 1 shows the block diagram of the proposed noise-shaped D/A convertor. The upper portion of the diagram depicts an ordinary delta-sigma modulator realised with the error-feedback structure, whereas the lower portion depicts the element selection logic. The two blocks are drawn in a manner which emphasises their similarity.

The modulator block accepts a finely quantised signal u and produces a coarsely quantised signal v. Denoting the quantiser error by e and adopting the convention that upper case variables represent Z-transforms, the output of the modulator is:

$$V = U + H_1 E \tag{1}$$

Thus, the output of the modulator is equal to its input plus an error term which, by suitable choice of H_1, can be designed to have a small magnitude in a selected frequency range. For the purpose of this discussion, assume that v is quantised to one of the $m+1$ integers in $[0, m]$.

At each time step n, the element selection logic determines which $v(n)$ of the m unit elements will be used to form the analogue output value. The output of the selection logic is $sv(n)$, a $1 \times m$ vector containing $v(n)$ ones and $m-v(n)$ zeros. Each unit element in the D/A convertor is controlled by a specific component of sv, so the output of the D/A convertor will be an analogue version of $v(n)$ plus an error term due to element mismatch. The function of the selection logic is to ensure that the error term has a noise-shaped spectrum.

The selection vector sv is computed in a manner analogous to that which produces v, except that many signals in the selection logic circuitry (those shown with heavy lines) are vector-valued. Based on the element usage requirement v, and on the contents of the vector sy, the vector quantiser sets certain elements of sv to one. The error of this quantisation operation se is fed back through an array of filters and added to the scalar-valued selection logic input su to form subsequent samples of sy. Thus, the output of the selection logic is

$$SV = SU[1 \ldots 1] + H_2(SE) \tag{2}$$

Let e_d be a (fixed) $m \times 1$ vector containing the difference between the value of each unit element in the D/A convertor and the mean of all the elements. Since the error between the actual output of the D/A convertor and its ideal output is $sv \cdot e_d$ and since the sum of all the components of e_d is zero by definition, the D/A convertor error is

$$\begin{aligned}(SU[1 \ldots 1] + H_2(SE))e_d &= SU \cdot 0 + H_2(SE)e_d \\ &= H_2(SE \cdot e_d)\end{aligned} \tag{3}$$

Eqn. 3 shows that static D/A convertor errors are shaped by the transfer function H_2, provided, of course, that the se signal is bounded. This result is independent of the su input signal, the operation of the vector quantiser and, most importantly, the errors in the unit elements.

However, the su input sequence, the value of H_2 and the quantiser algorithm affect the magnitude of the se signal. Since a vector quantiser of the form shown in Fig. 1 is more complex than a simple binary quantiser, proving the stability of the selection logic is a much more difficult problem than proving the stability of a delta-sigma modulator. The latter problem is unsolved and is usually addressed by simulation. In this Letter, simulations are likewise used to determine the stability of the selection logic.

Simulation results: The simulation results reported here use different H_1 and H_2 filters but identical algorithms for generating the su input and implementing the vector quantiser. To minimise the magnitude of the sy vector while keeping all components positive, su is taken as the negative of the minimum of the output of the H_2–1 filter. To minimise the magnitude of the se vector, the vector quantiser sets those components of sv to one that correspond to the v largest components of sy. No claim is made that the preceding design choices are optimal. A better vector quantiser strategy might involve using all the state information in the H_2–1 block rather than just its output.

Fig. 2 shows output spectra for a third-order lowpass modulator which uses the preceding strategies together with a 16 element D/A convertor and several different H_2 filters. The unit elements in the D/A were subject to fixed random errors having a standard deviation of 1% whereas the input was a half-scale sinewave located at the bandedge for an oversampling ratio of 64. The curves exhibit the 0, 20, 40 and 60dB/decade slopes characteristic

of zeroth, first, second and ideal third-order shaping. The first-order configuration is functionally identical to that of [2] and thus is guaranteed stable with a maximum *sy* value of 1. The second-order configuration is at best conditionally stable; the simulation exhibited a maximum *sy* value of 6. The fact that *sy* is larger for second-order shaping than for first-order shaping accounts for the observation that there is a significant difference between the two only if the oversampling ratio is > 30.

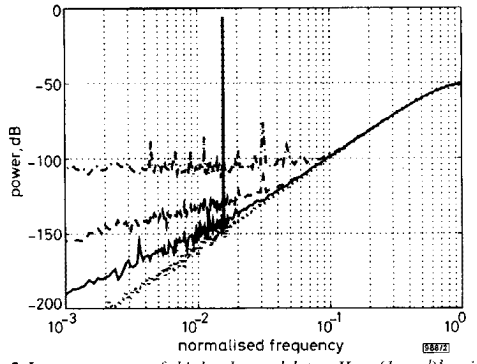

Fig. 2 *Lowpass spectra of third-order modulator, $H_1 = (1 - z^{-1})^3$, using 16 element D/A convertor and supplied with half-scale sinewave input*

— - — 1% element mismatch, no shaping
— — 1% element mismatch, shaped by $H_2(z) = (1 \quad z^{-1})$
——— 1% element mismatch, shaped by $H_2(z) = (1 - z^{-1})^2$
- - - - ideal D/A convertor

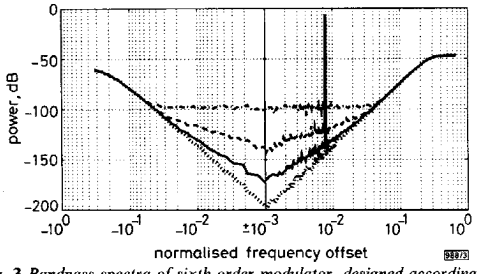

Fig. 3 *Bandpass spectra of sixth-order modulator, designed according to [4] with $||H_1||_\infty = 8$, using 16 element D/A convertor and supplied with half-scale sinewave input*

— - — 1% element mismatch, no shaping
— — 1% element mismatch, shaped by $H_2(z) = (1 - z^{-1} + z^{-2})$
——— 1% element mismatch, shaped by fourth-order transfer function designed according to [4] with $||H_2||_\infty = 2$
- - - - ideal D/A convertor

Fig. 3 shows output spectra for a sixth-order bandpass modulator under similar conditions. Once again, the systems are stable and the slopes are consistent with the order of H_2. The bandpass system with a second-order H_2 exhibited a peak *sy* value of 2, whereas the use of a fourth-order H_2 yielded a peak *sy* value of 3.5. Once again, the higher-order shaping only provides a significant advantage when the oversampling ratio is moderately high. With the exception of the last example, all the H_2 functions presented in this Letter are FIR with integer coefficients. Although such filters greatly simplify the selection logic, the architecture does not require their use.

Conclusions: A method for noise-shaping the error caused by element mismatch in a unit-element D/A convertor was demonstrated with simulations. Example systems yielding first and second-order shaping in a lowpass modulator and second- and fourth-order shaping in a bandpass modulator were presented. As is necessary for high order delta-sigma modulators, the stability of the high order versions of the algorithm is determined by the simulations.

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56 byte optical cell selection at 55 Gbit/s in bit-interleave multiplexing photonic ATM switch

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Indexing terms: Nonlinear optical loop mirrors, Chalcogenide glasses

Experiments on selecting 56 byte optical cells out of a four-channel bit-interleave multiplexed 55 Gbit/s pulse stream are carried out using a nonlinear optical loop mirror (NOLM) including a chalcogenide glass fibre.

Introduction: In the future B-ISDN, optical technologies are expected to play an important role not only in transmission but also in network functions such as switching and routing, to efficiently accommodate the continuously increasing demand for bandwidth and flexibility [1]. We have previously proposed a new photonic ATM switch based on a bit-interleave multiplexing scheme [2]. Because this switch uses a bit-interleave multiplexing scheme, the hardware complexity is minimal and synchronisation can be maintained by using optical PLL techniques [3]. Furthermore, ultrafast optical devices such as nonlinear optical loop mirrors (NOLM) developed for ultrahigh speed optical demultiplexing can be used [3]. As a result, it should be possible to select cells out of high speed optical pulse stream of >100 Gbit/s.

In this switch, the pulses (bits) of cells appear cyclically in the aggregate pulse stream during a time slot corresponding to a cell length because cells from each input channel are bit-interleave multiplexed. Thus, an optical cell selection module (OCSM) for selecting desired cells on a slot-by-slot basis at each output becomes an important function [2]. For example, when an all-optical switch such as an NOLM is used for high speed selection in the OCSM, the timing of control pulses must be set up on a slot-by-slot basis.

In this Letter, we report experimental results that confirm the function of the OCSM by demonstrating the selection of 56 byte optical cells out of a four-channel bit-interleave multiplexed 55 Gbit/s cell stream. Selection is achieved using a nonlinear optical loop mirror (NOLM) including a chalcogenide glass fibre. The switching of the cell selection was performed by tuning the optical path length of control pulses.

Configuration of OCSM: The configuration of the OCSM is shown in Fig. 1. The OCSM mainly consists of the NOLM, a synchronous circuit, and a tunable optical delay line module (TODL). The NOLM functions like a logical AND gate in which a signal pulse appears at the output only when it is gated by a control pulse. The essential component of the NOLM is the nonlinear optical fibre in which the Kerr effect is used to change the phase of the signal pulse. The control pulse stream is generated by another short pulse LD that has a different wavelength from that of the signal pulse stream. The synchronisation between the signal pulse and the control pulse in the NOLM can be maintained by using a synchronous circuit such as a PLL [3].

To select a cell belonging to the *i*th input channel (i = 1, 2, ...,